



FIG. 2

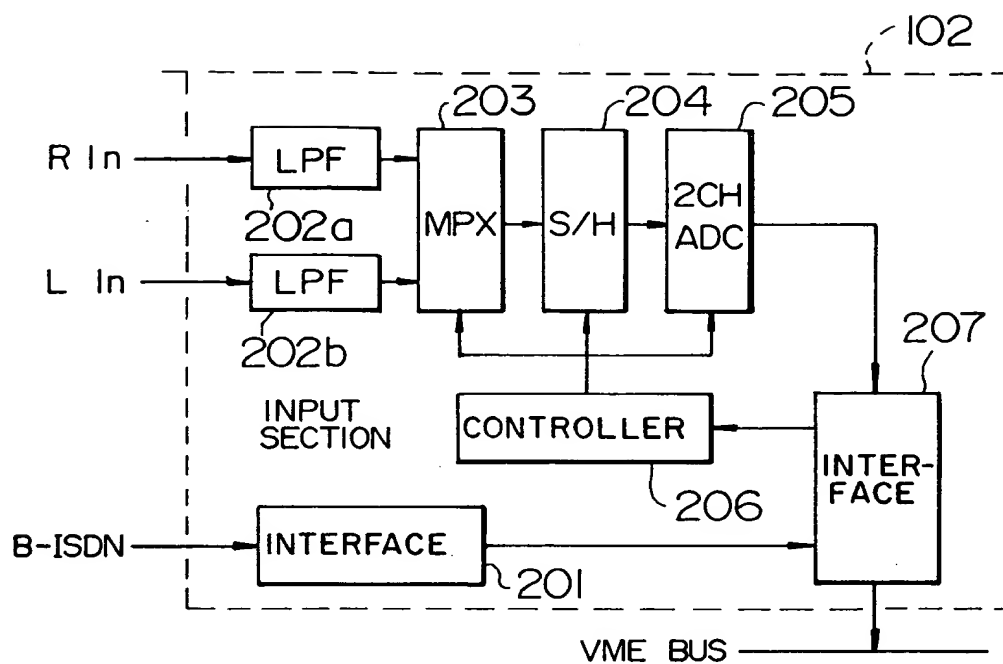
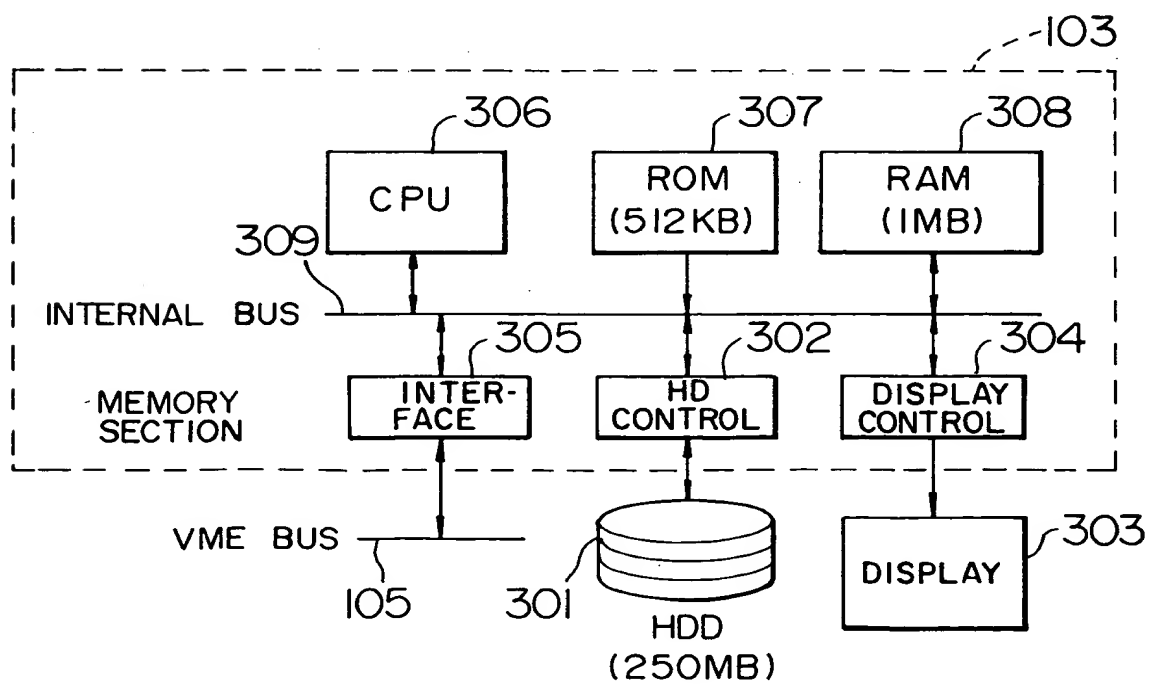


FIG. 3



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FIG. 4

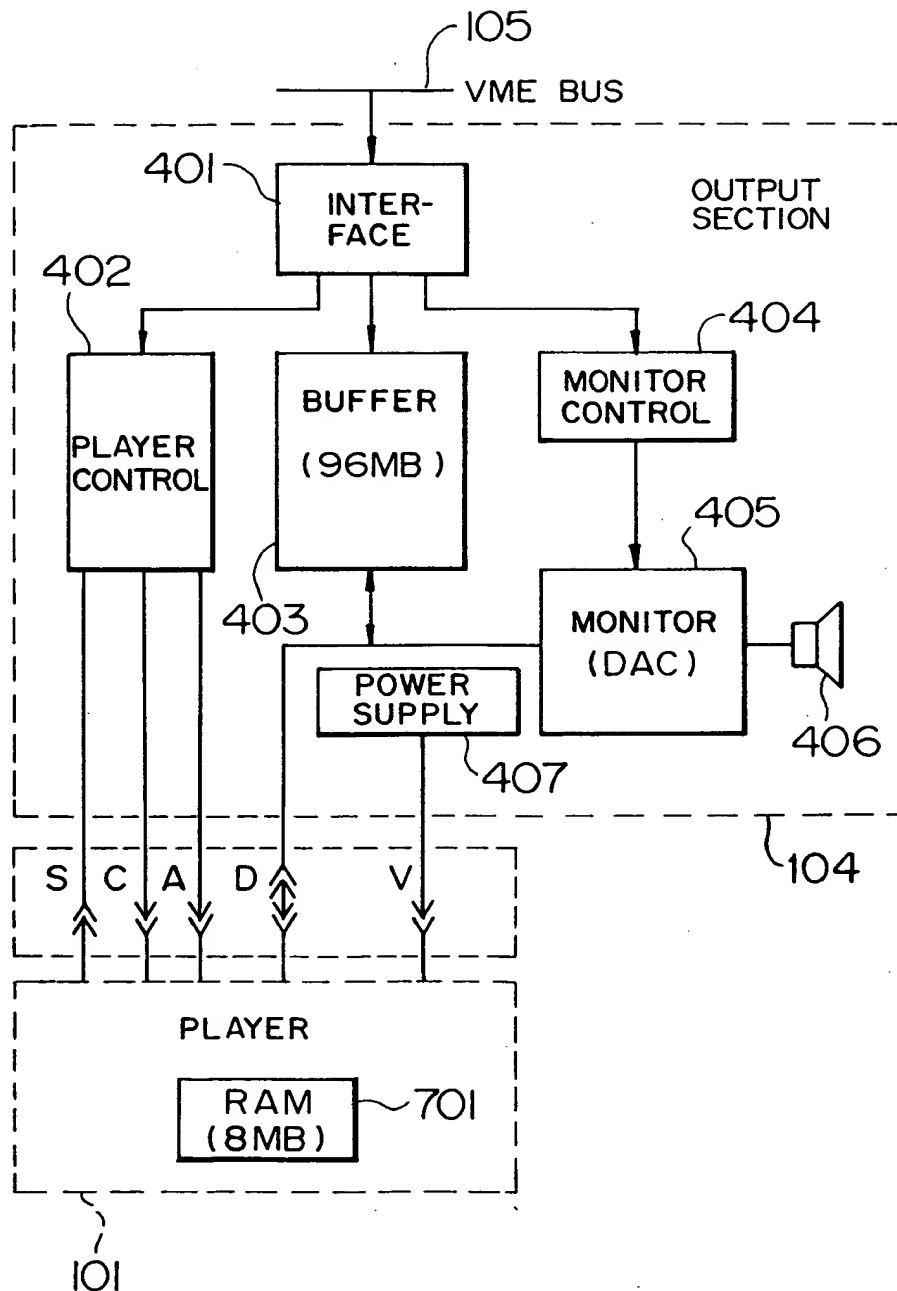


FIG. 5

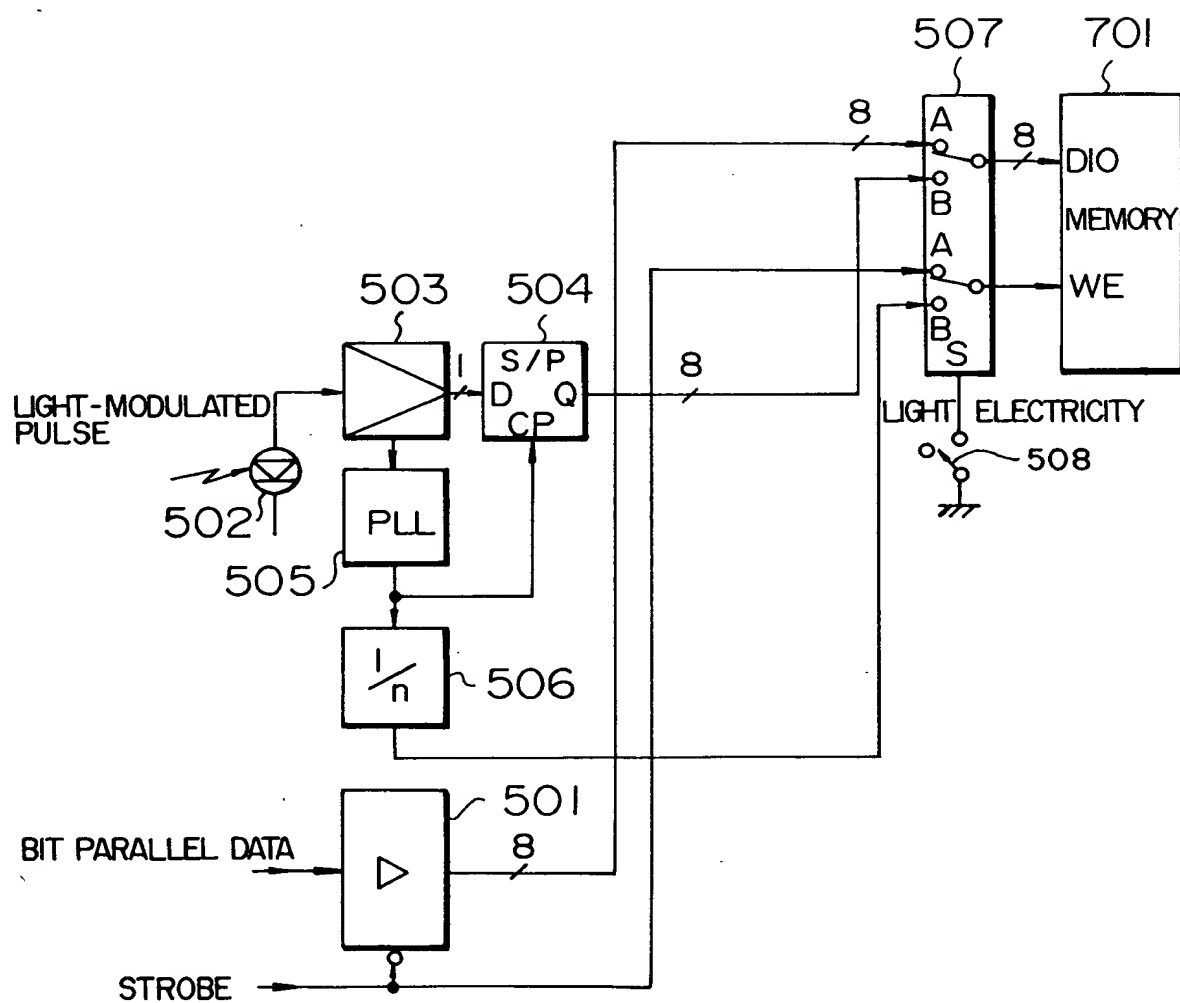
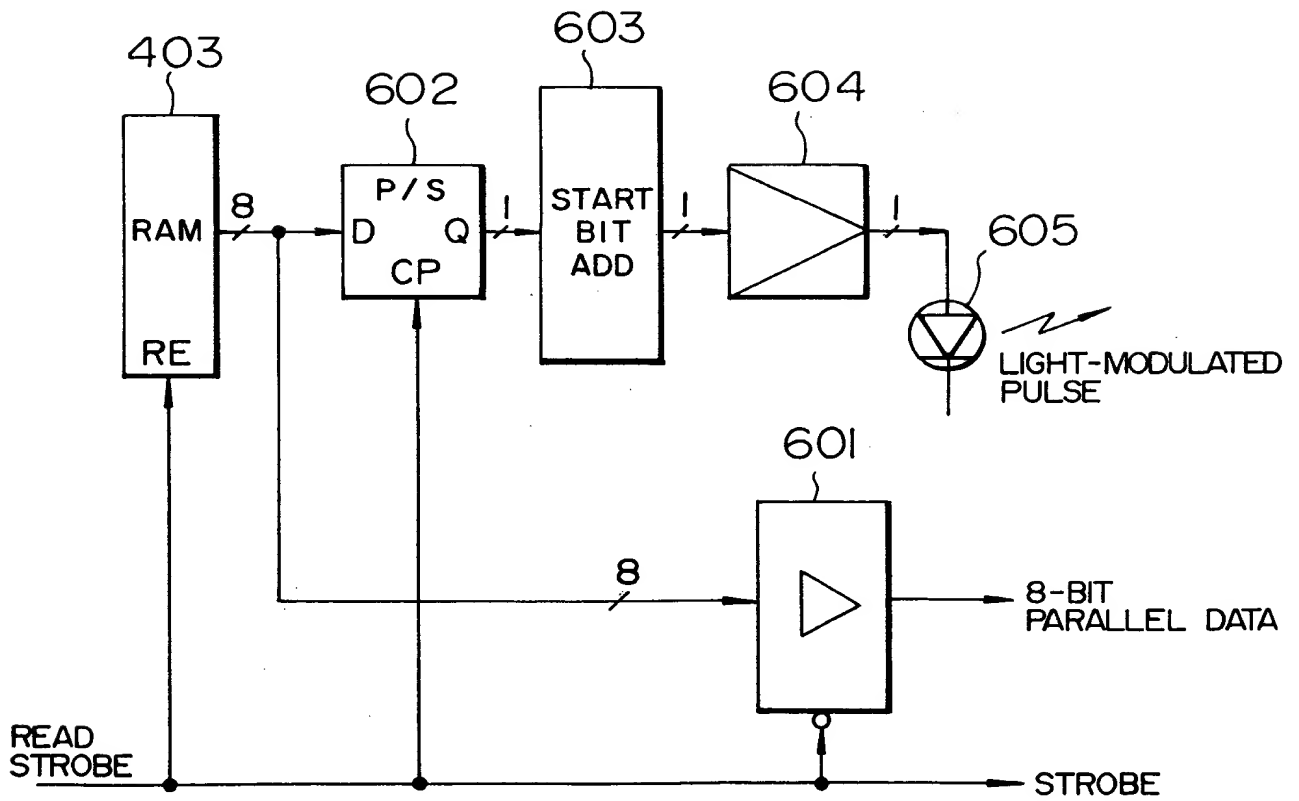


FIG. 6



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FIG. 8

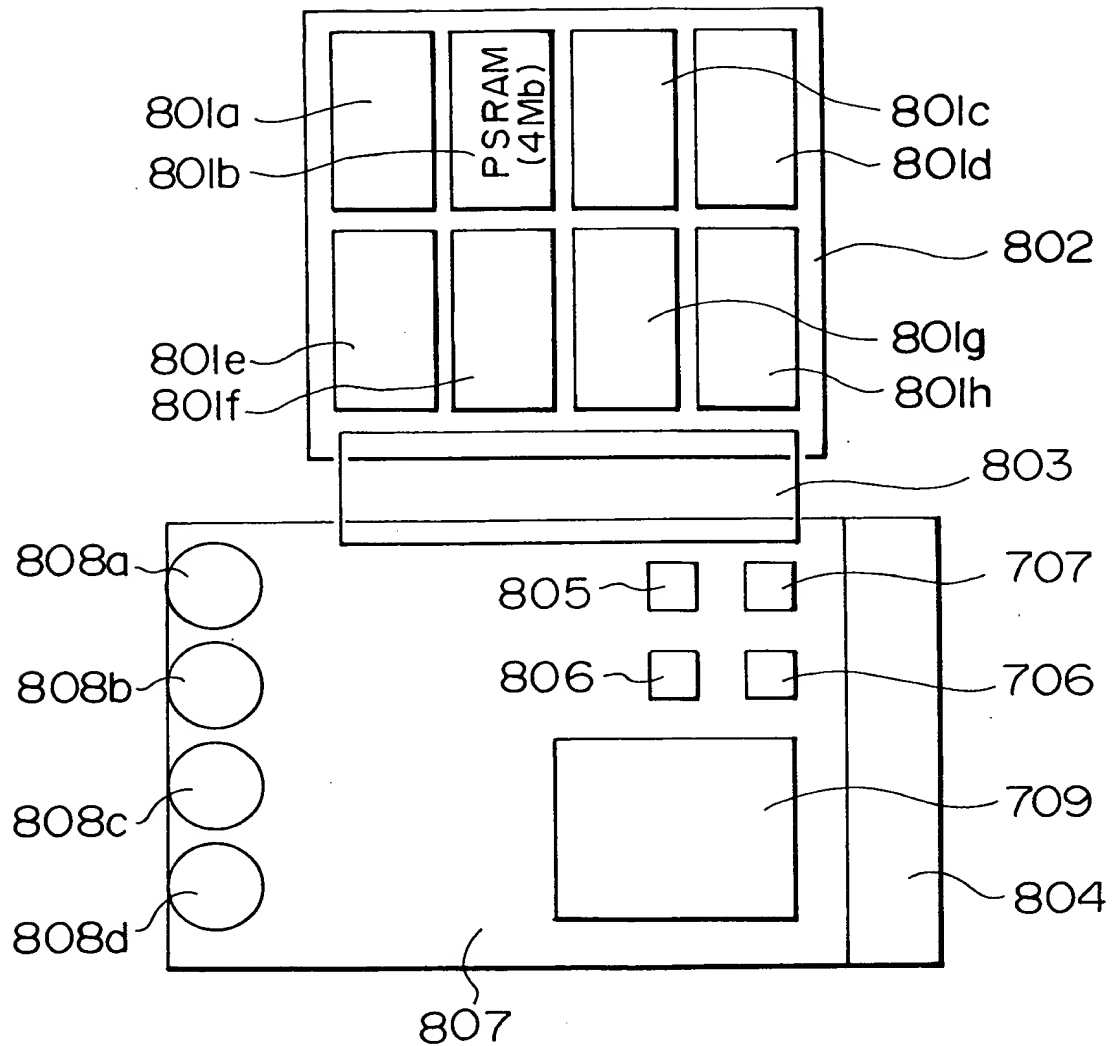
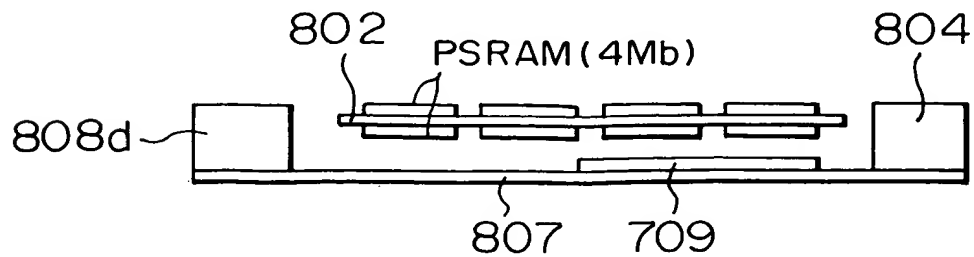


FIG. 9



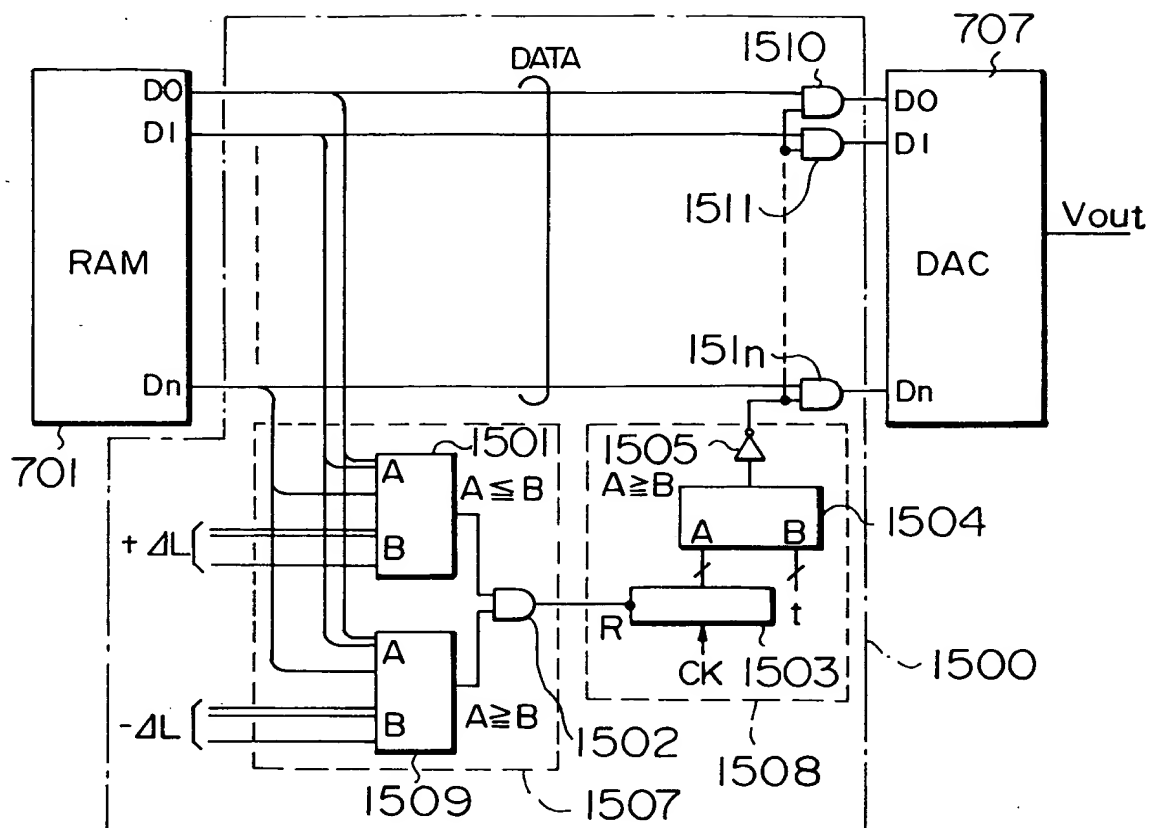








# FIG.15



# FIG.16

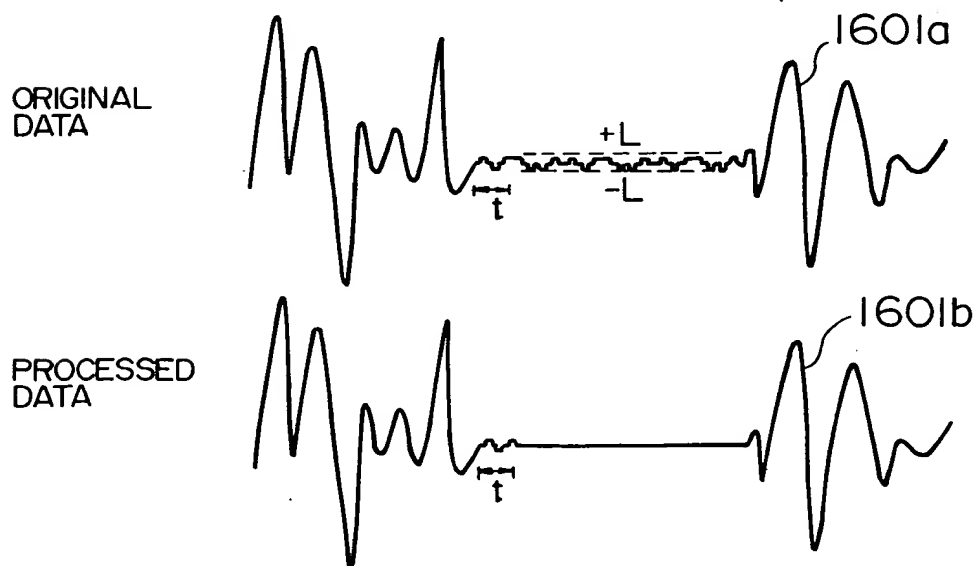




FIG. 19

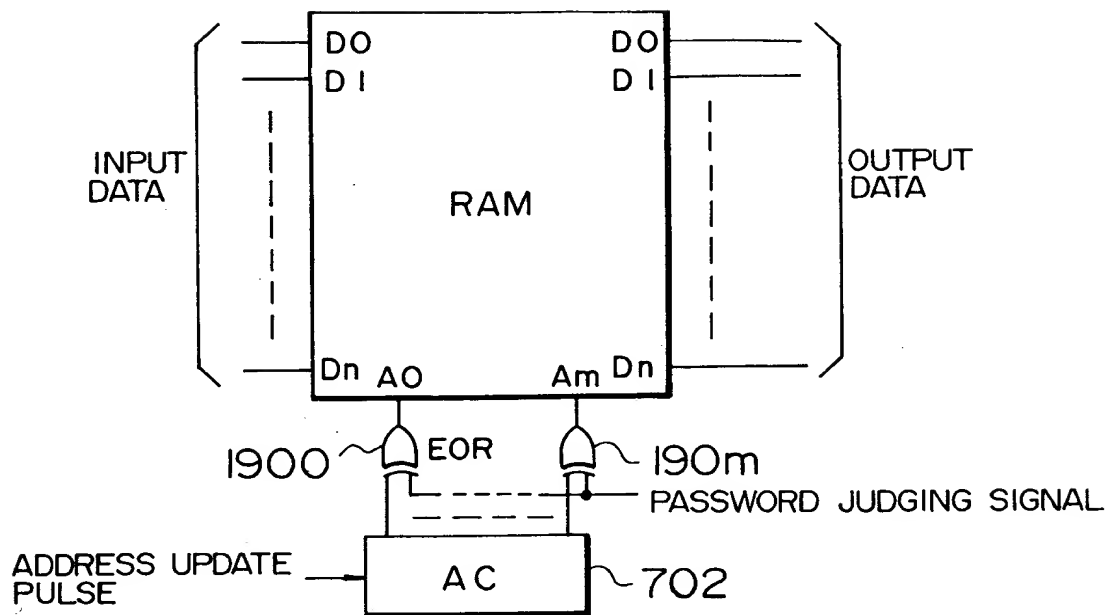


FIG. 20

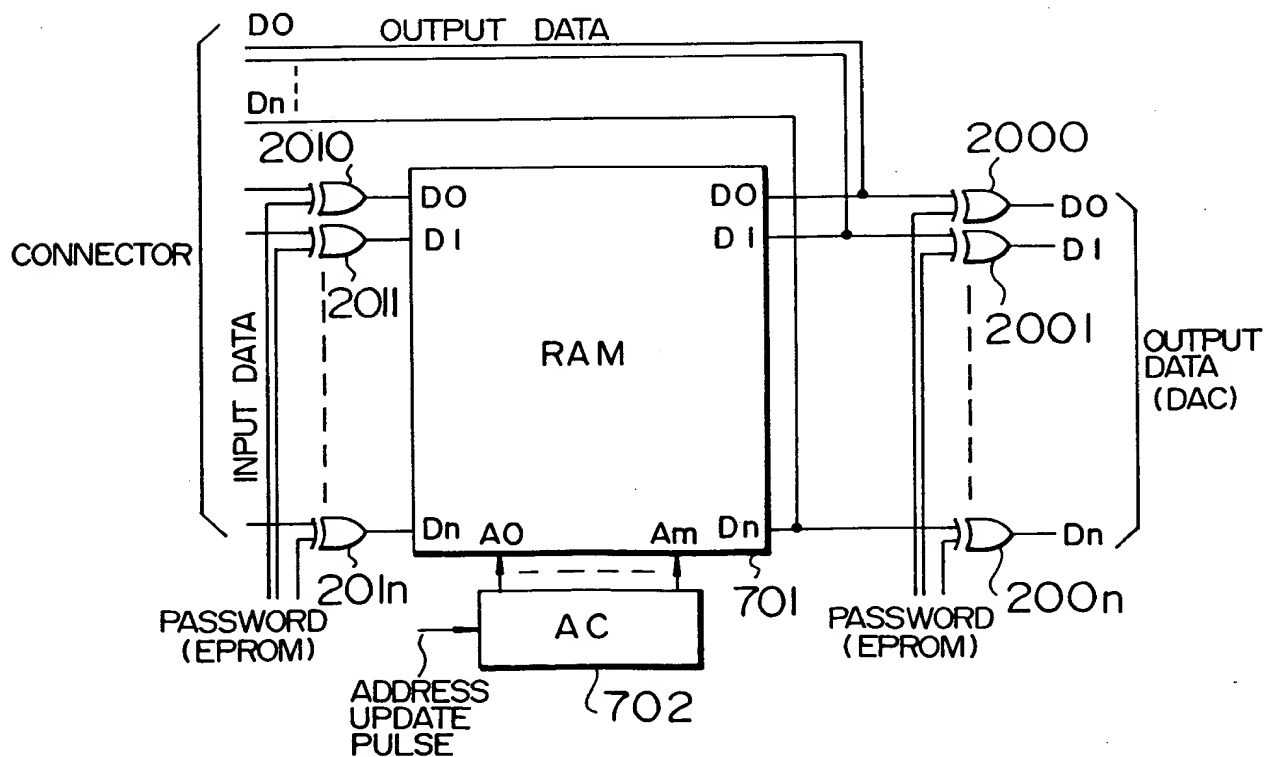


FIG. 21

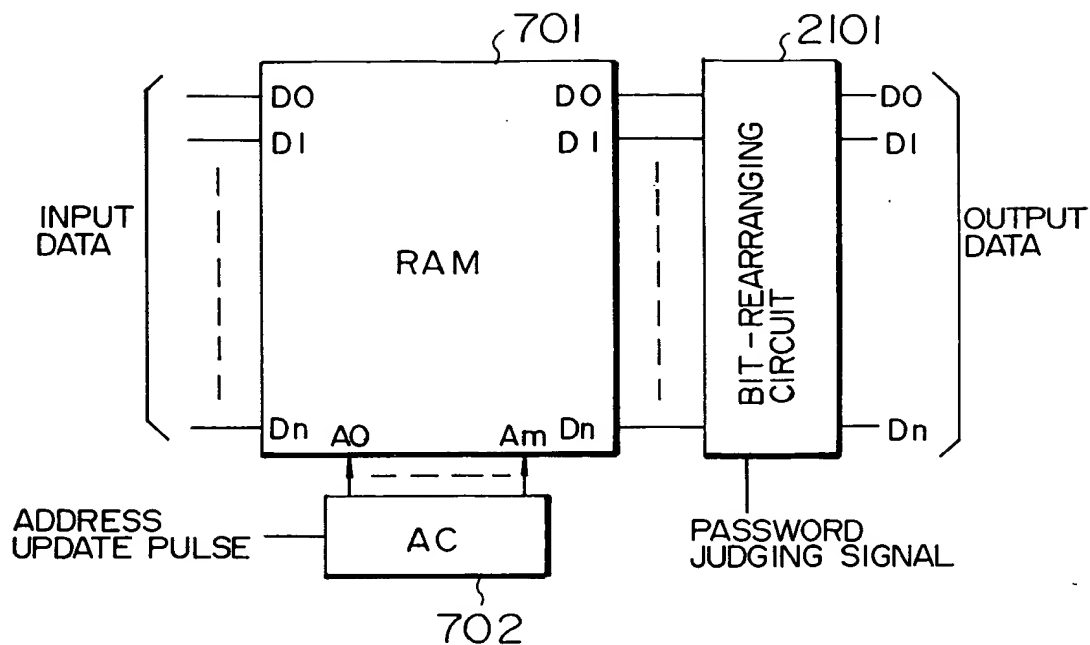
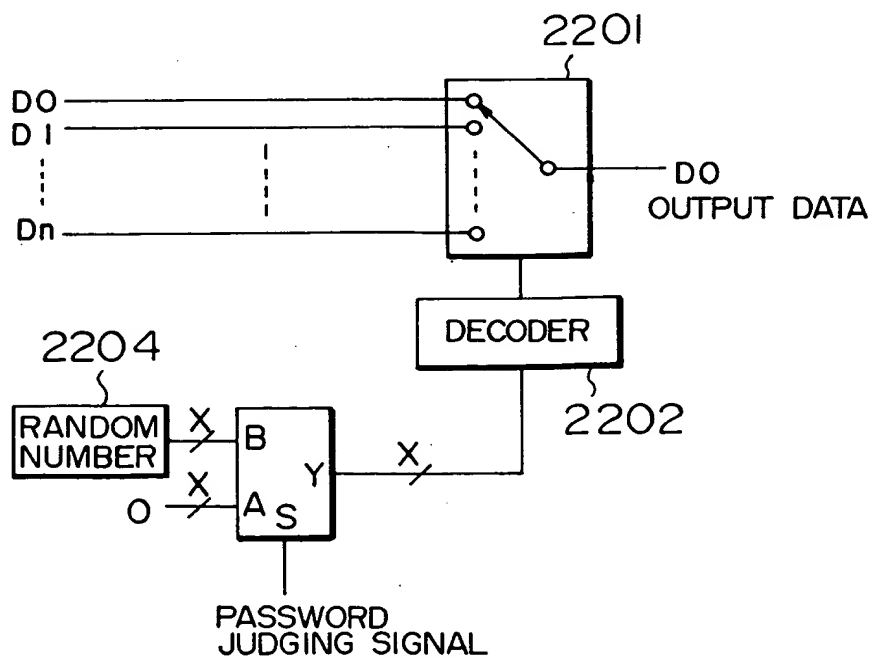
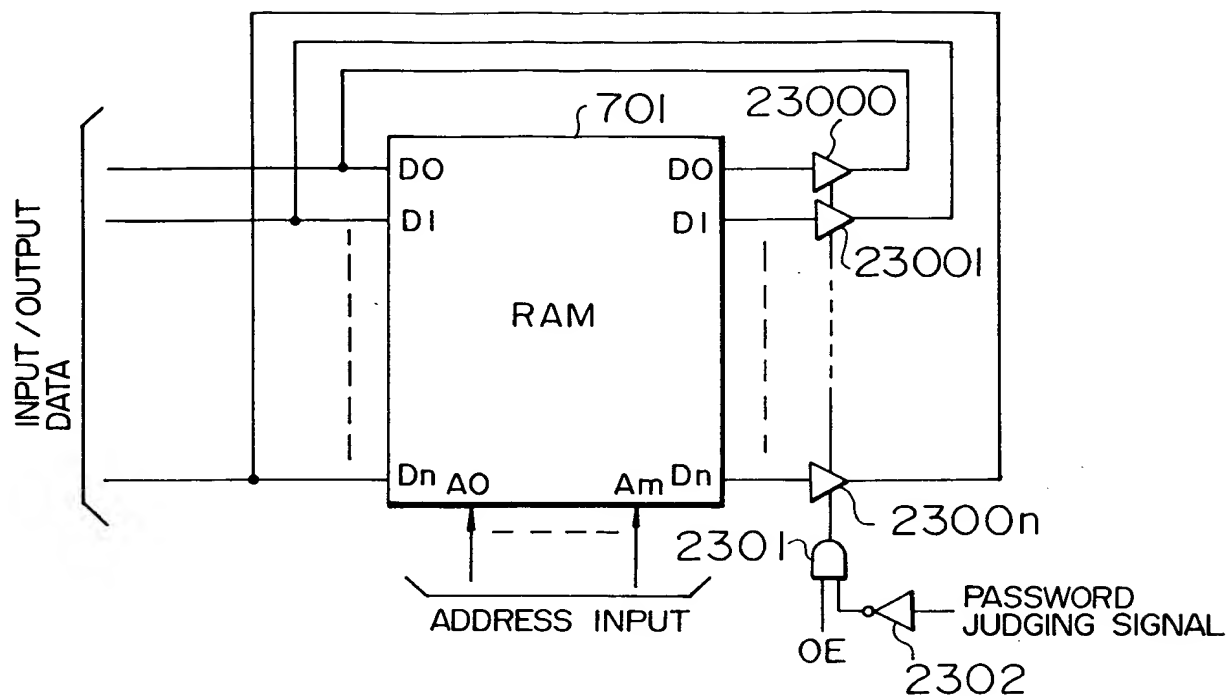


FIG. 22



# FIG. 23



# FIG. 24

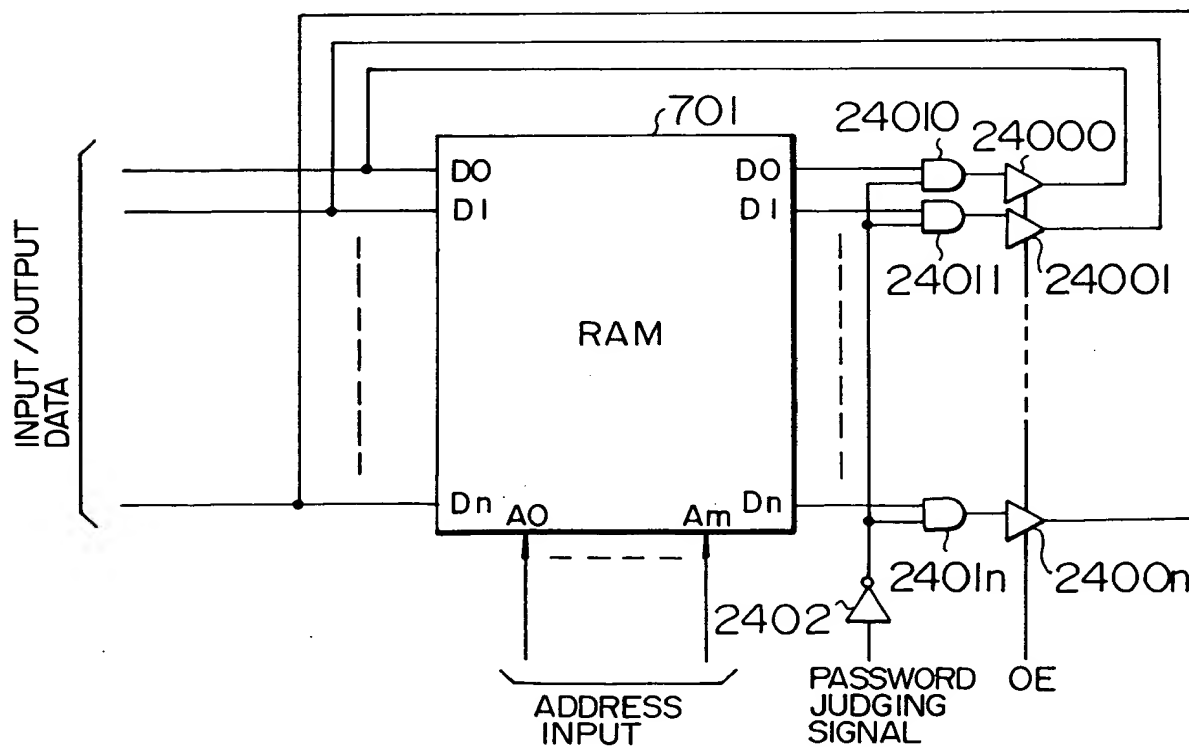






FIG. 26

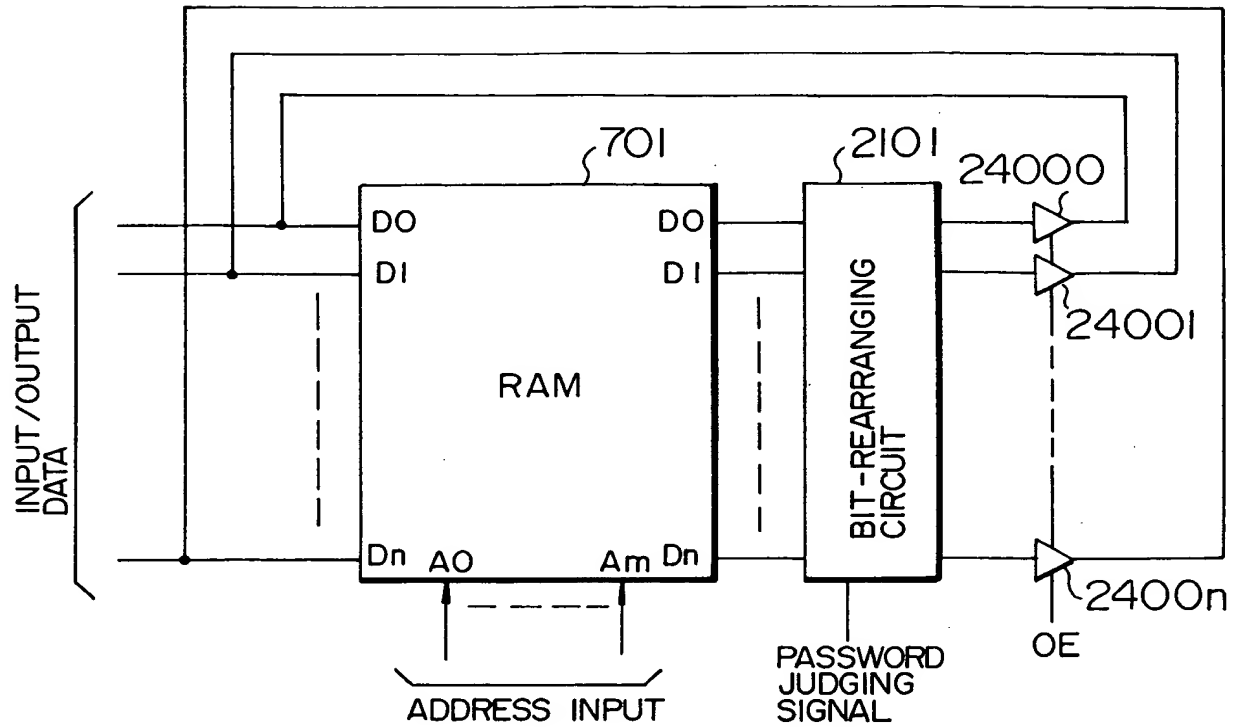


FIG. 27

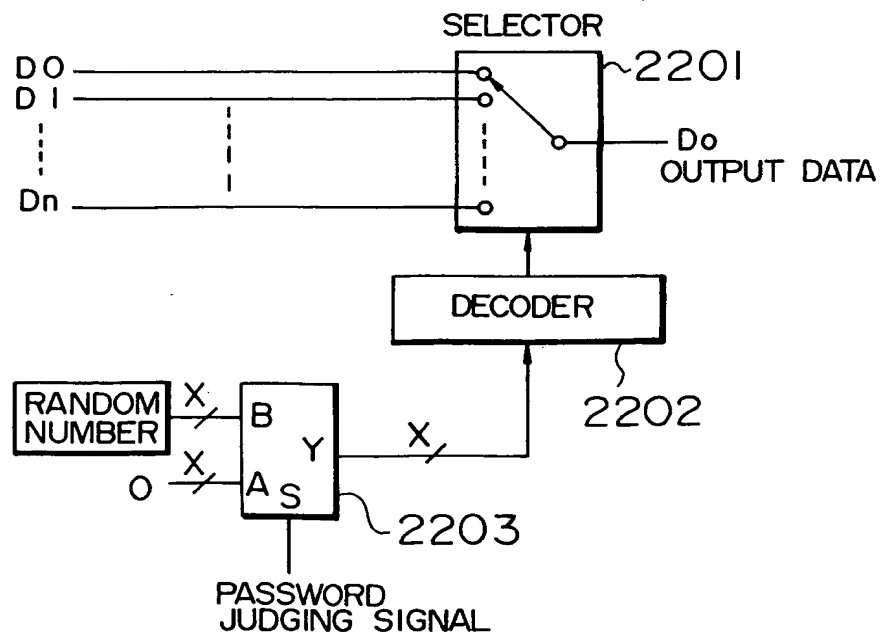


FIG. 28

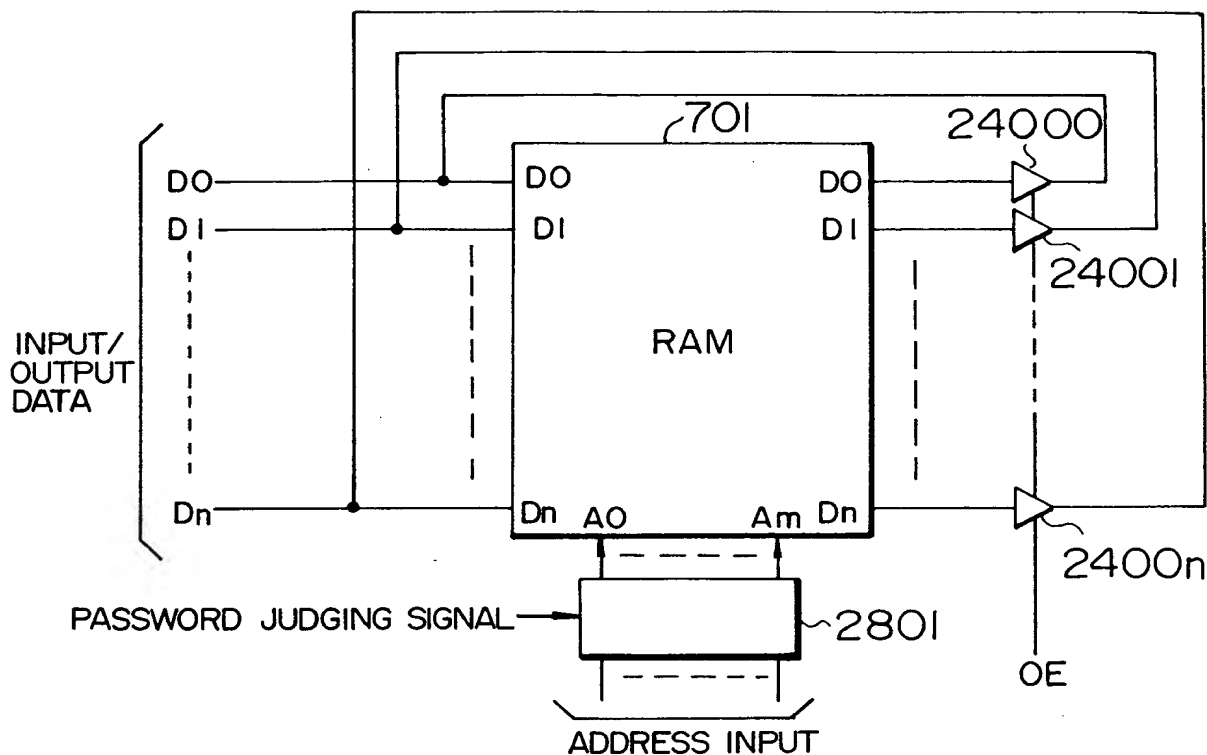


FIG. 29

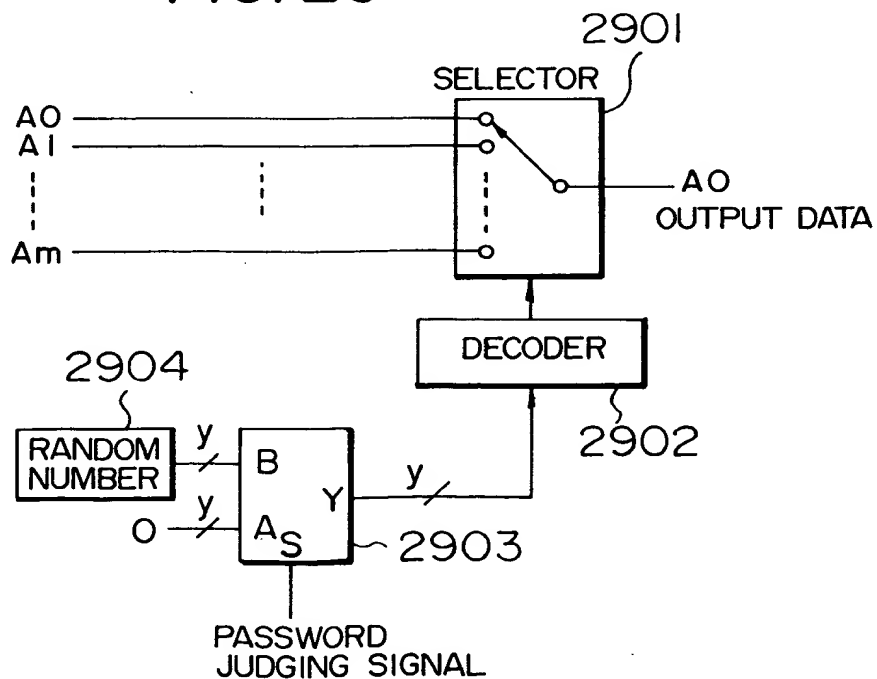


FIG. 30

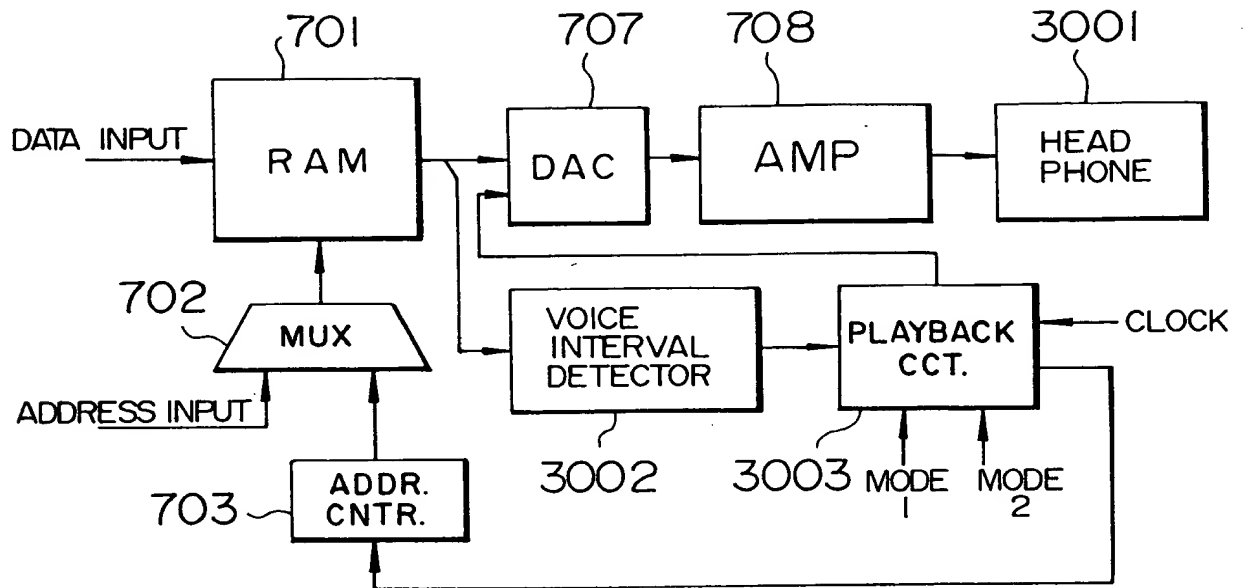
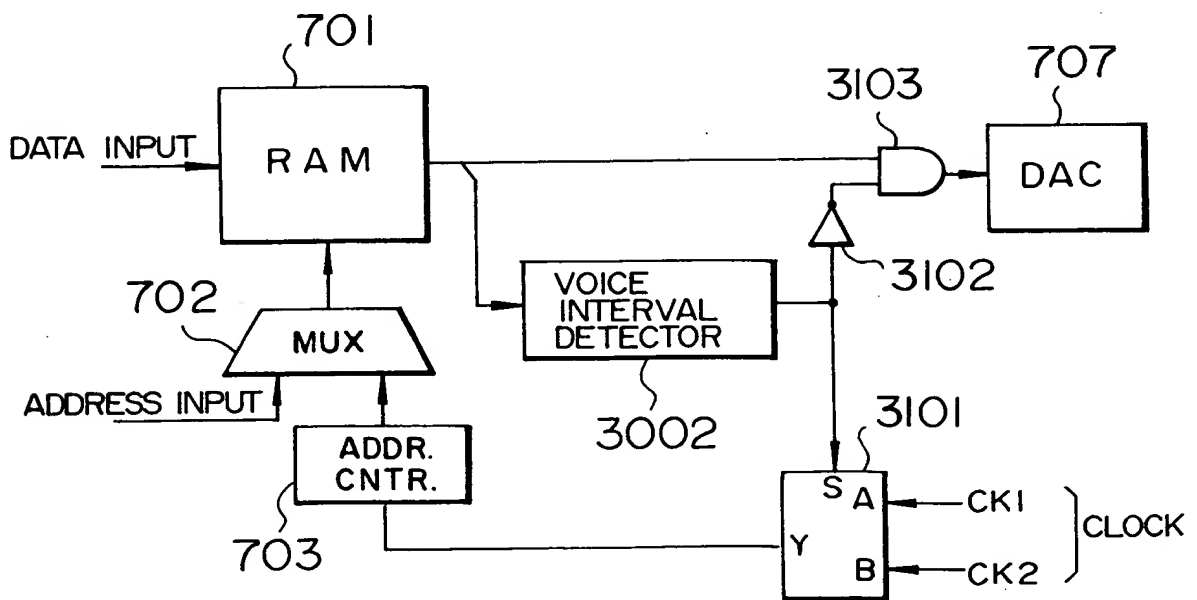


FIG. 31



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FIG. 32



FIG. 35

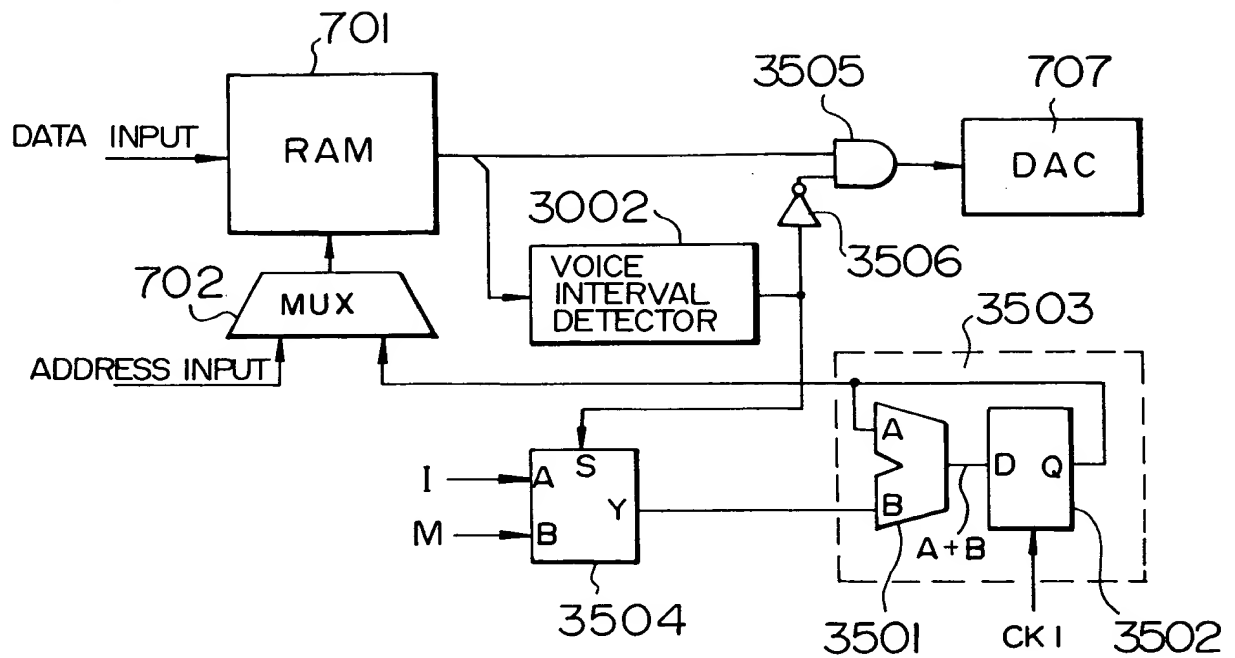


FIG. 36

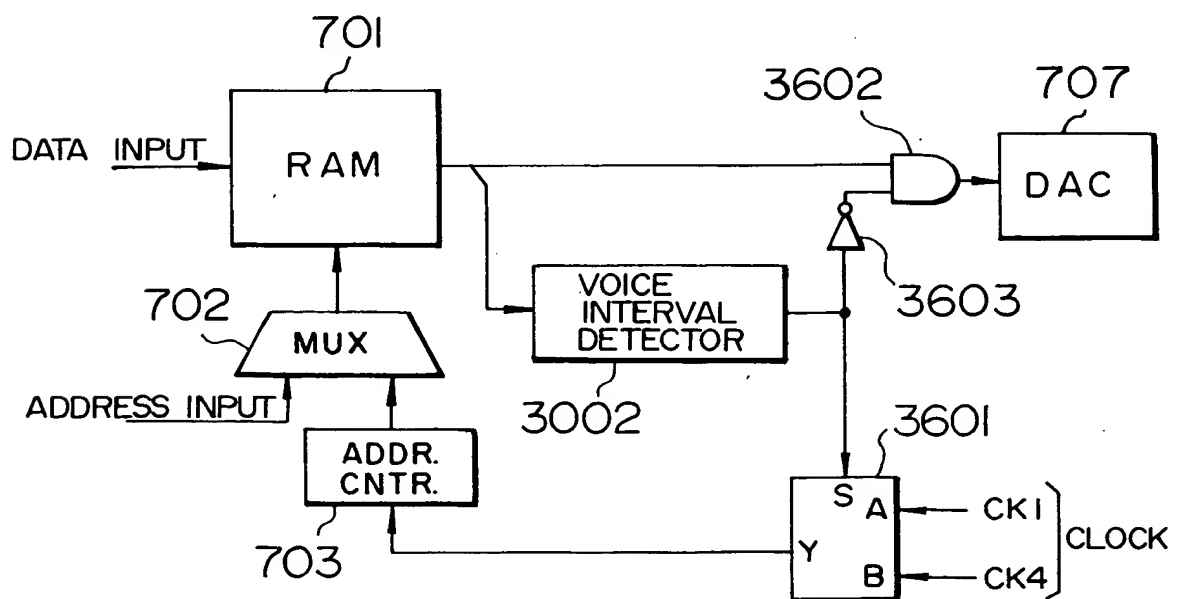


FIG. 37

FIG. 38

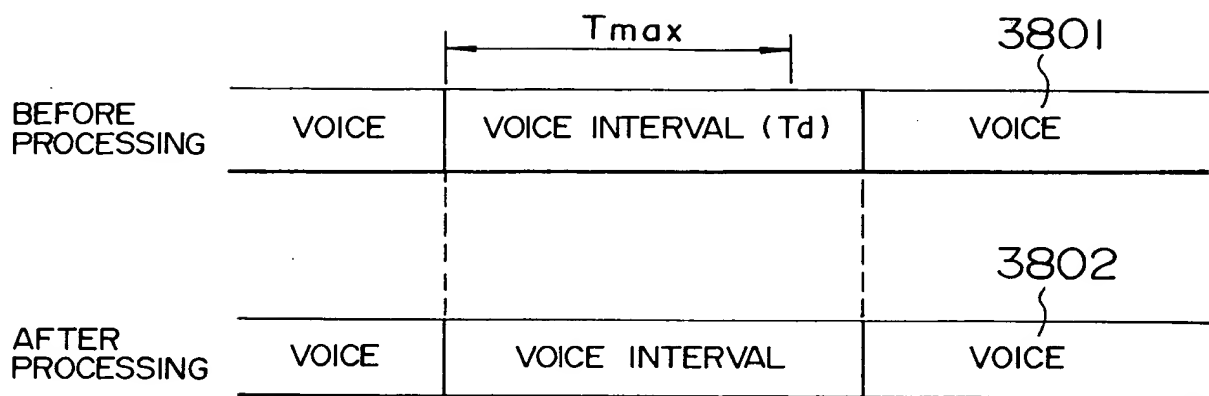


FIG. 39

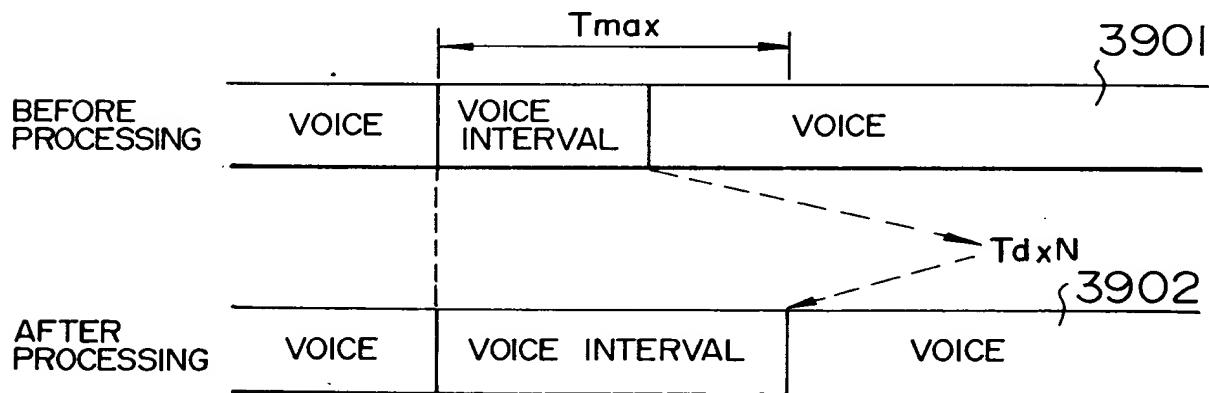


FIG. 40

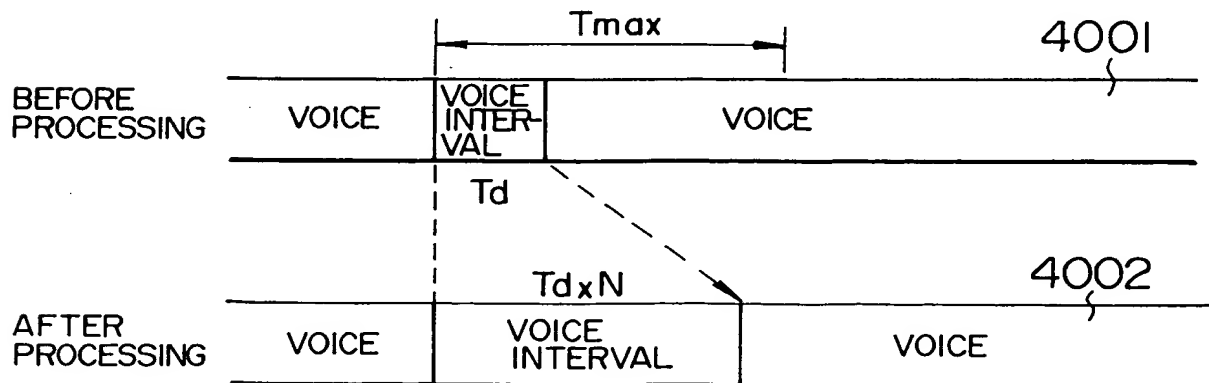




FIG. 41

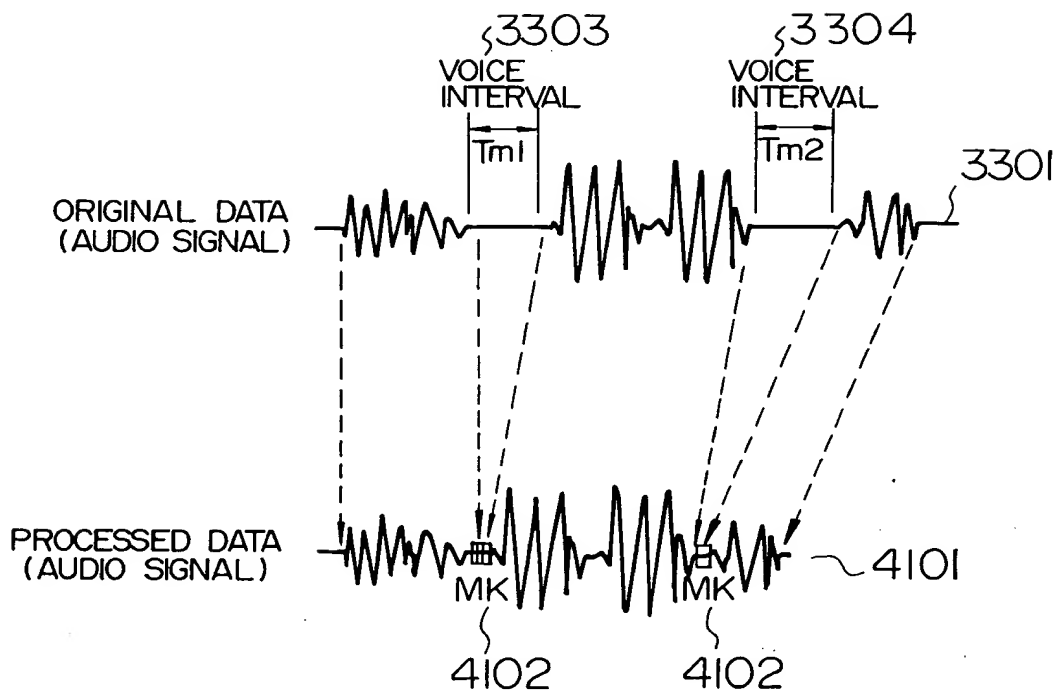


FIG. 42

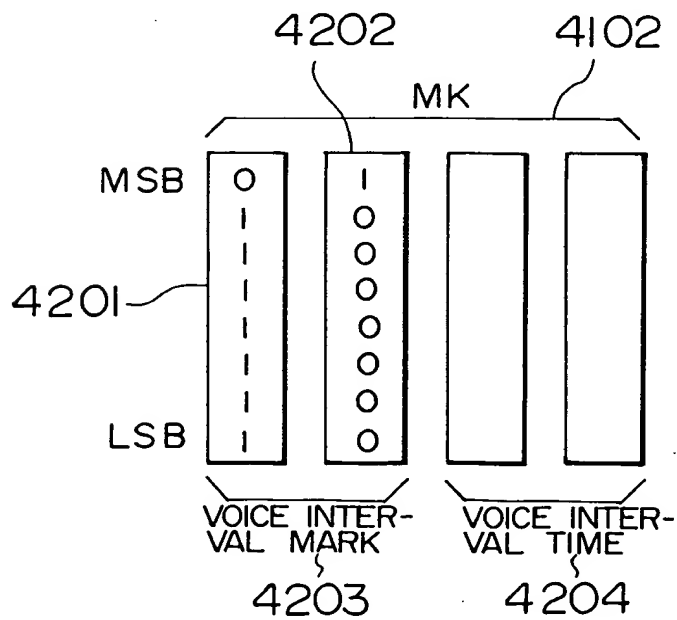


FIG. 43

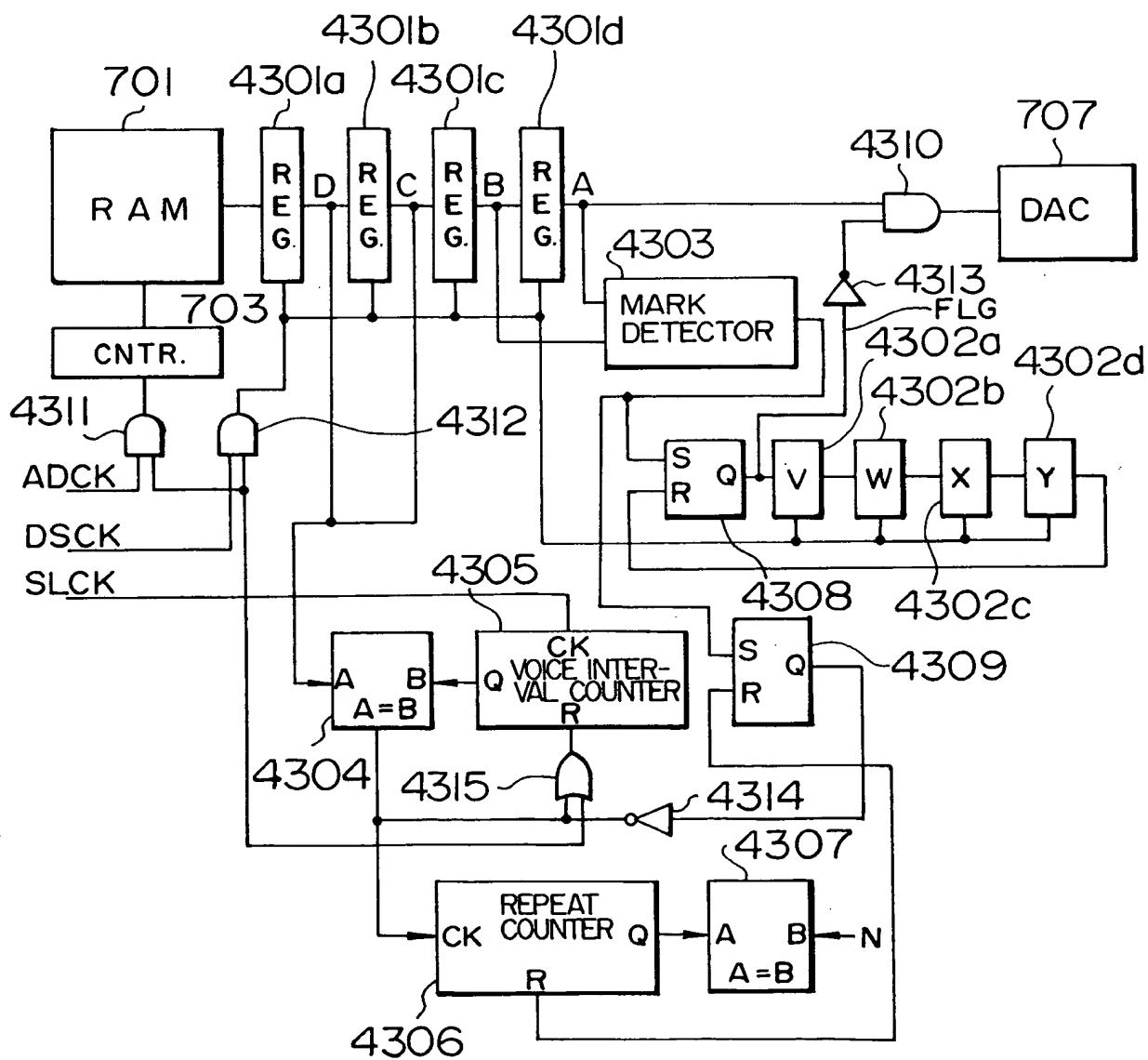
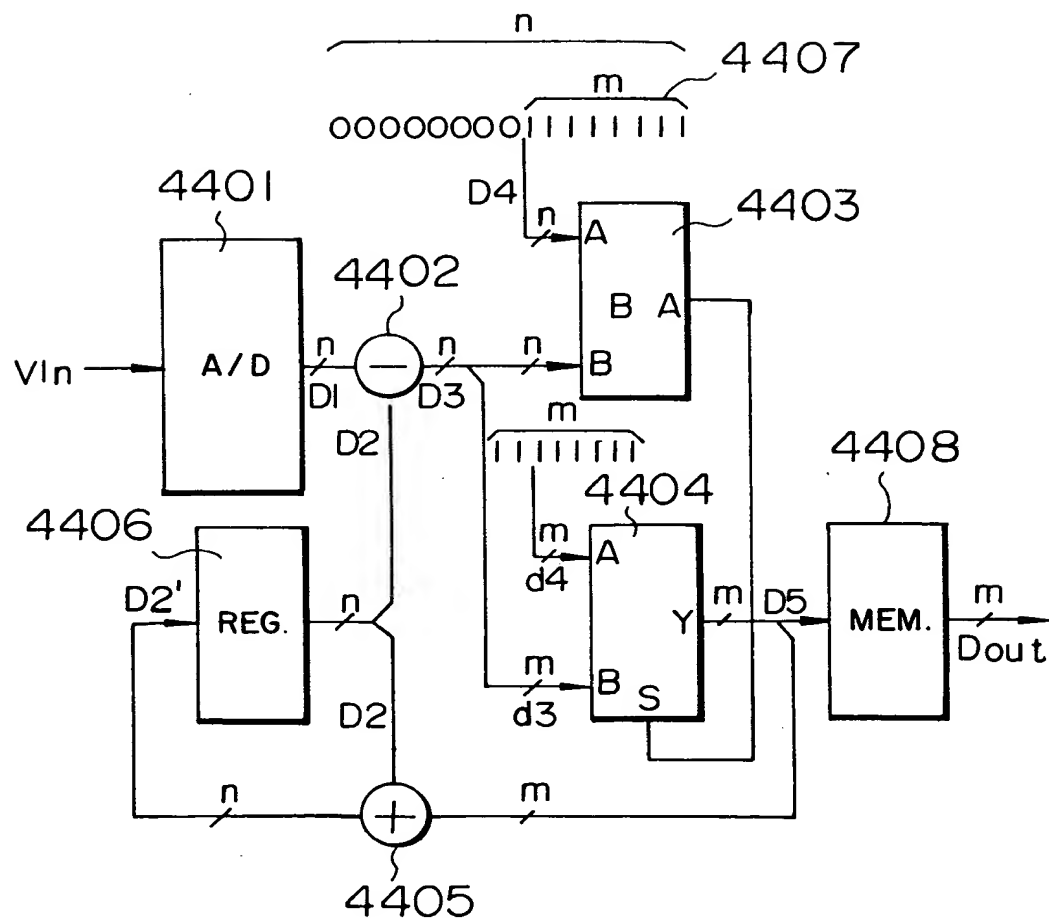


FIG. 44



The diagram shows a block labeled 4601 containing a MEM. block, a REG. block, and a D/A block. An input DIn enters the MEM. block. The MEM. block has an output path labeled m/d5 leading to a summing junction (circle with a plus sign). The summing junction also receives input from the REG. block and has an output path labeled n/D7 leading to the D/A block. The REG. block has an input path labeled n/D6 from the D/A block and an output path labeled n leading to the summing junction. The D/A block has an output V out.

FIG. 47

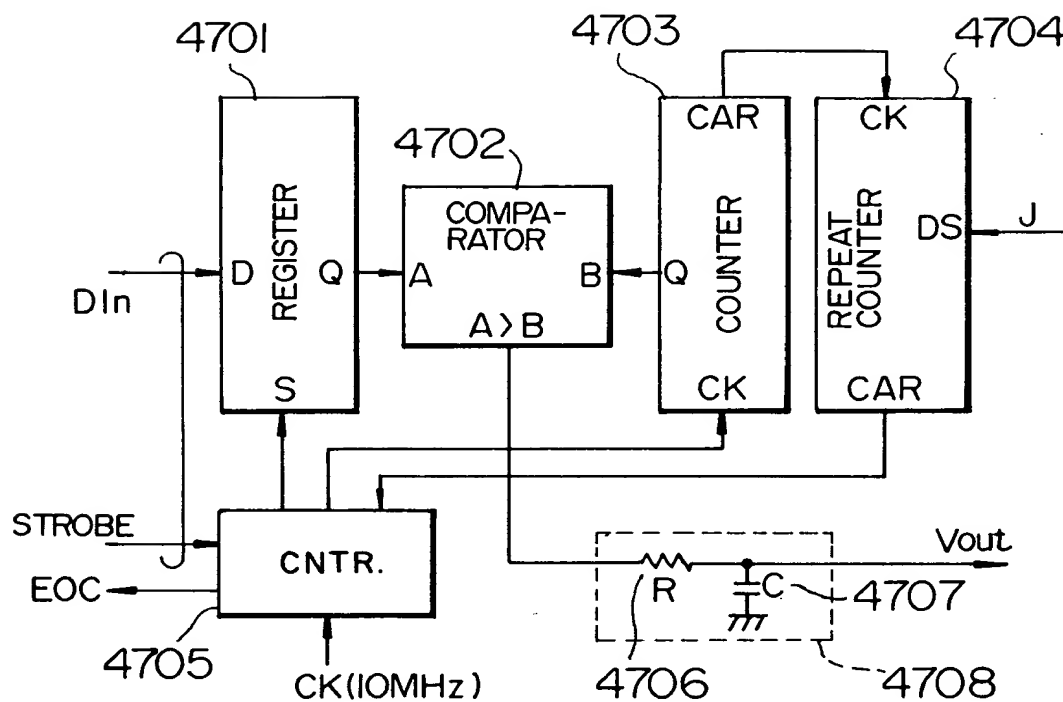


FIG. 48

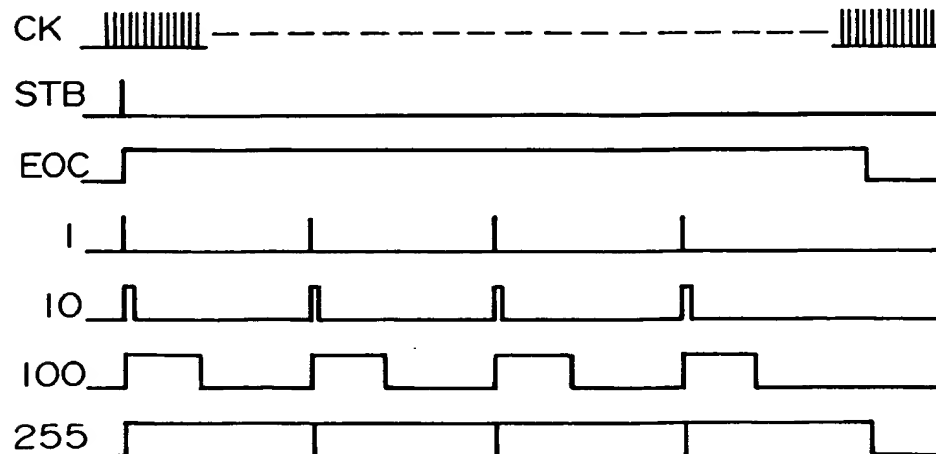
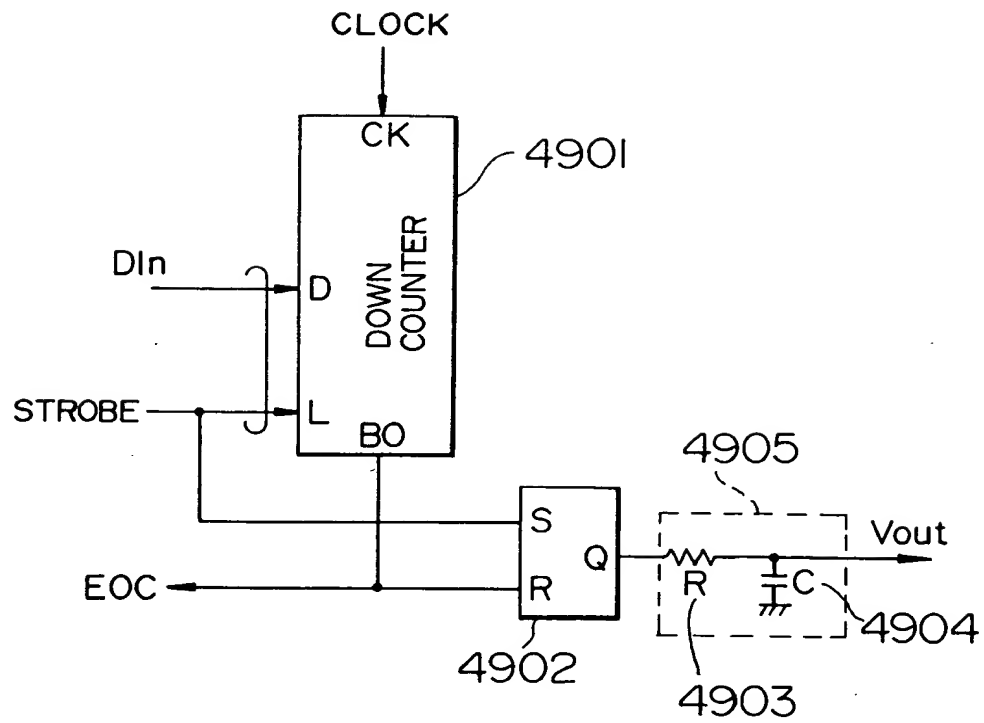


FIG. 49



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FIG. 51

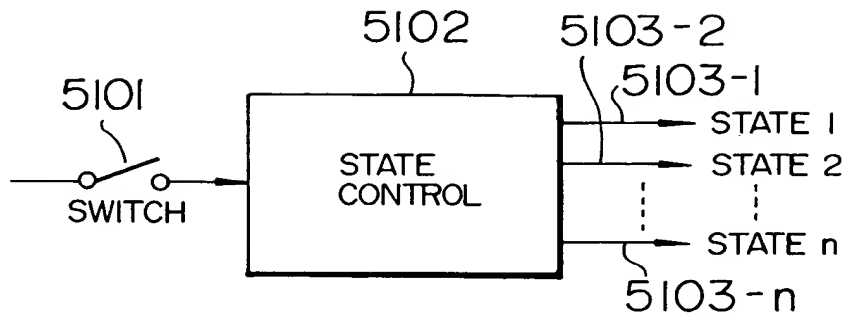


FIG. 52

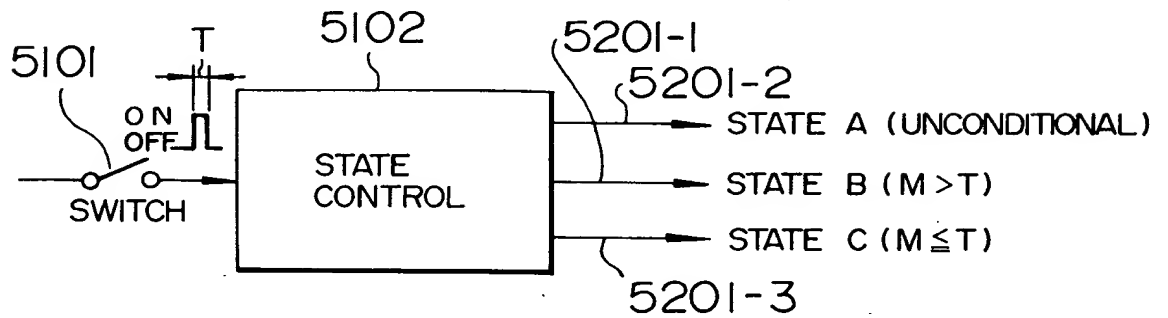


FIG. 53

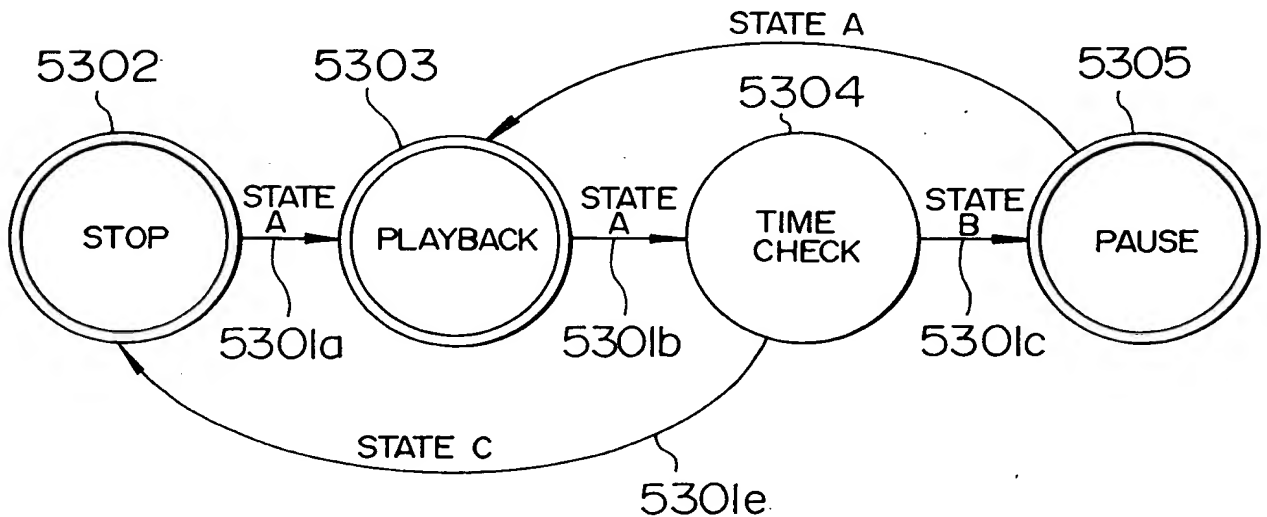




FIG. 54

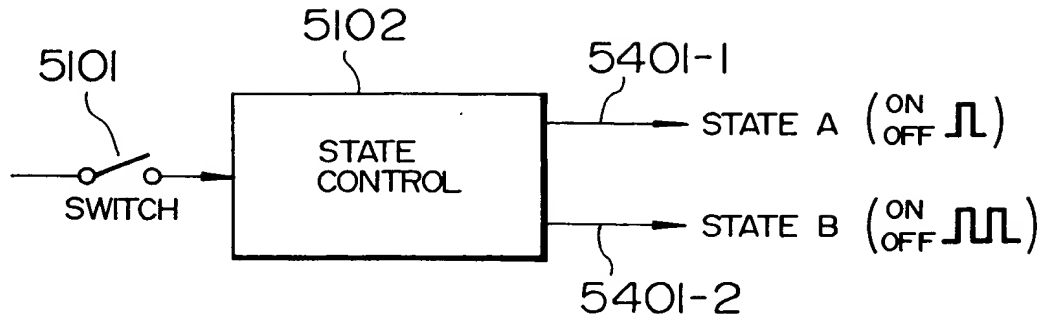
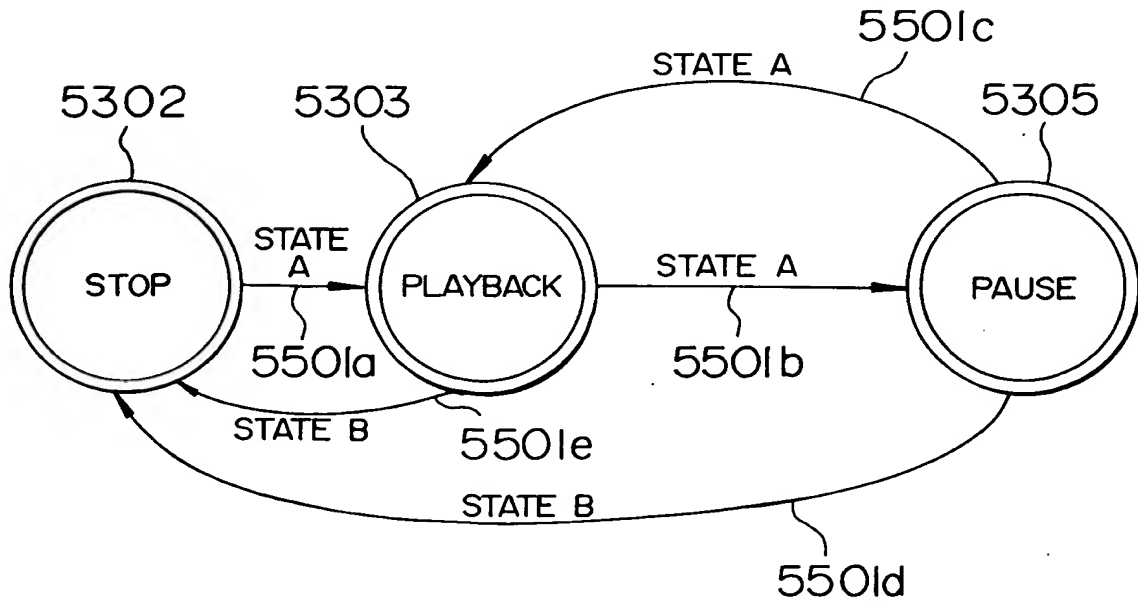
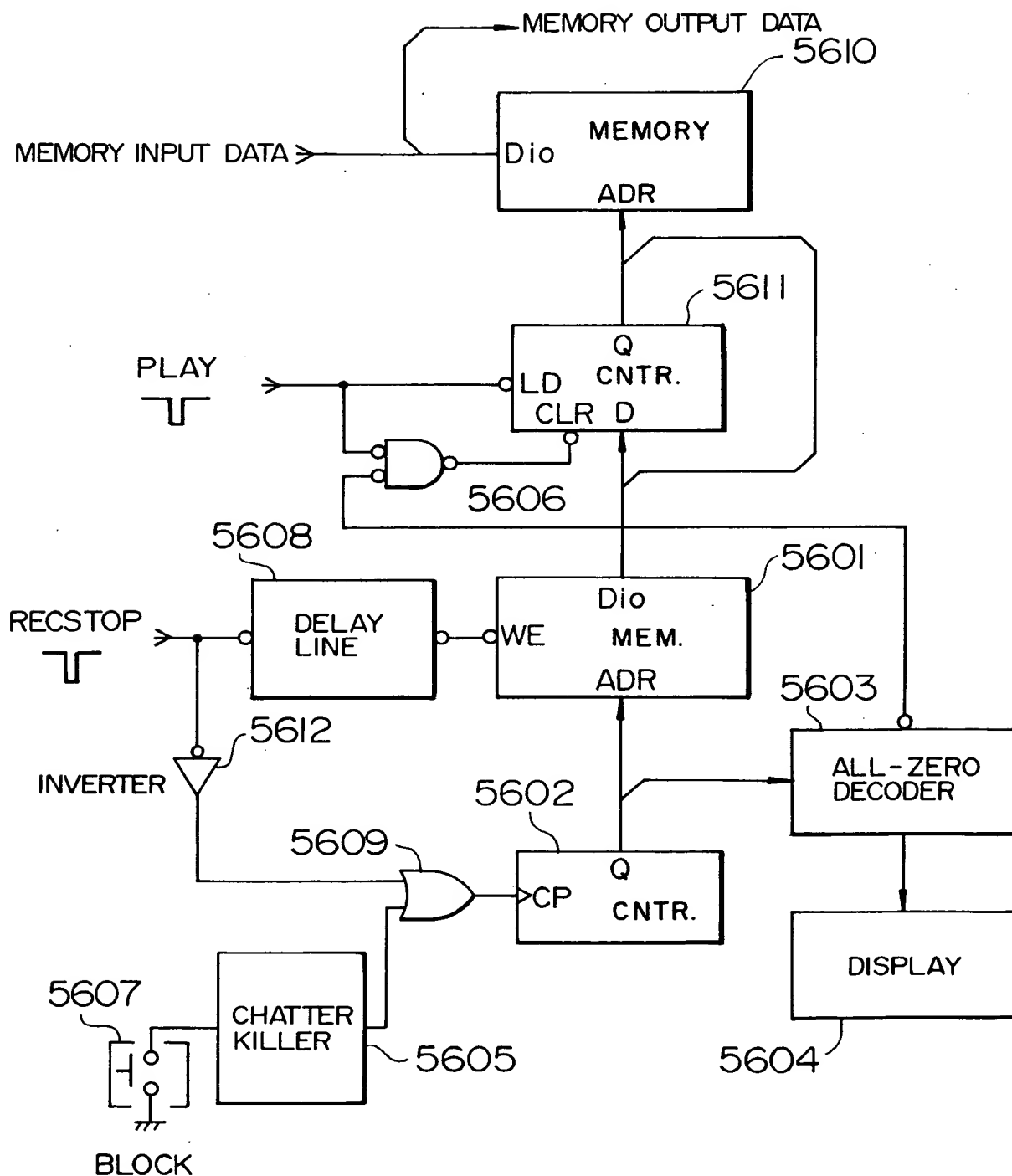


FIG. 55



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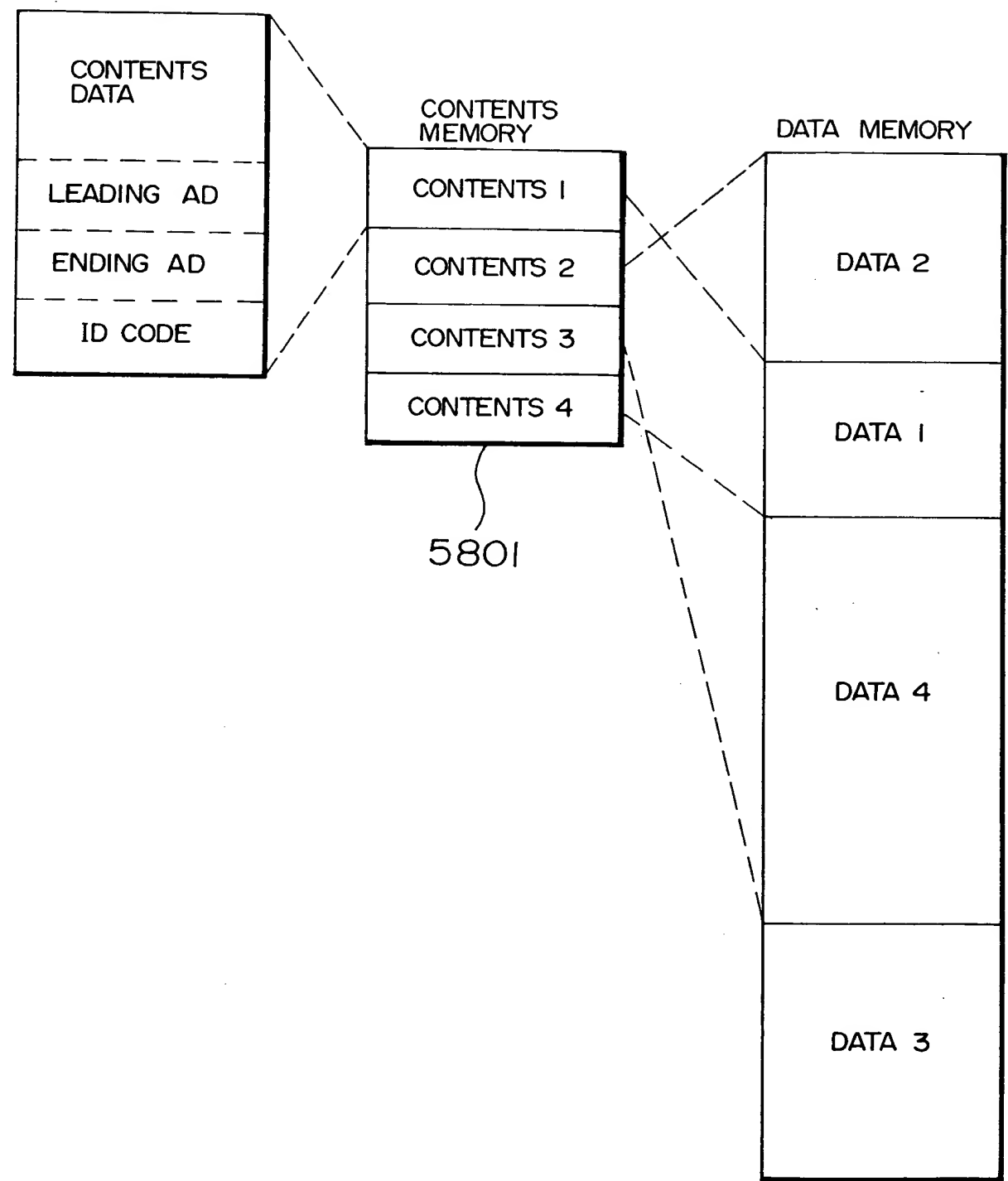
FIG. 56



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FIG. 58



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FIG. 59

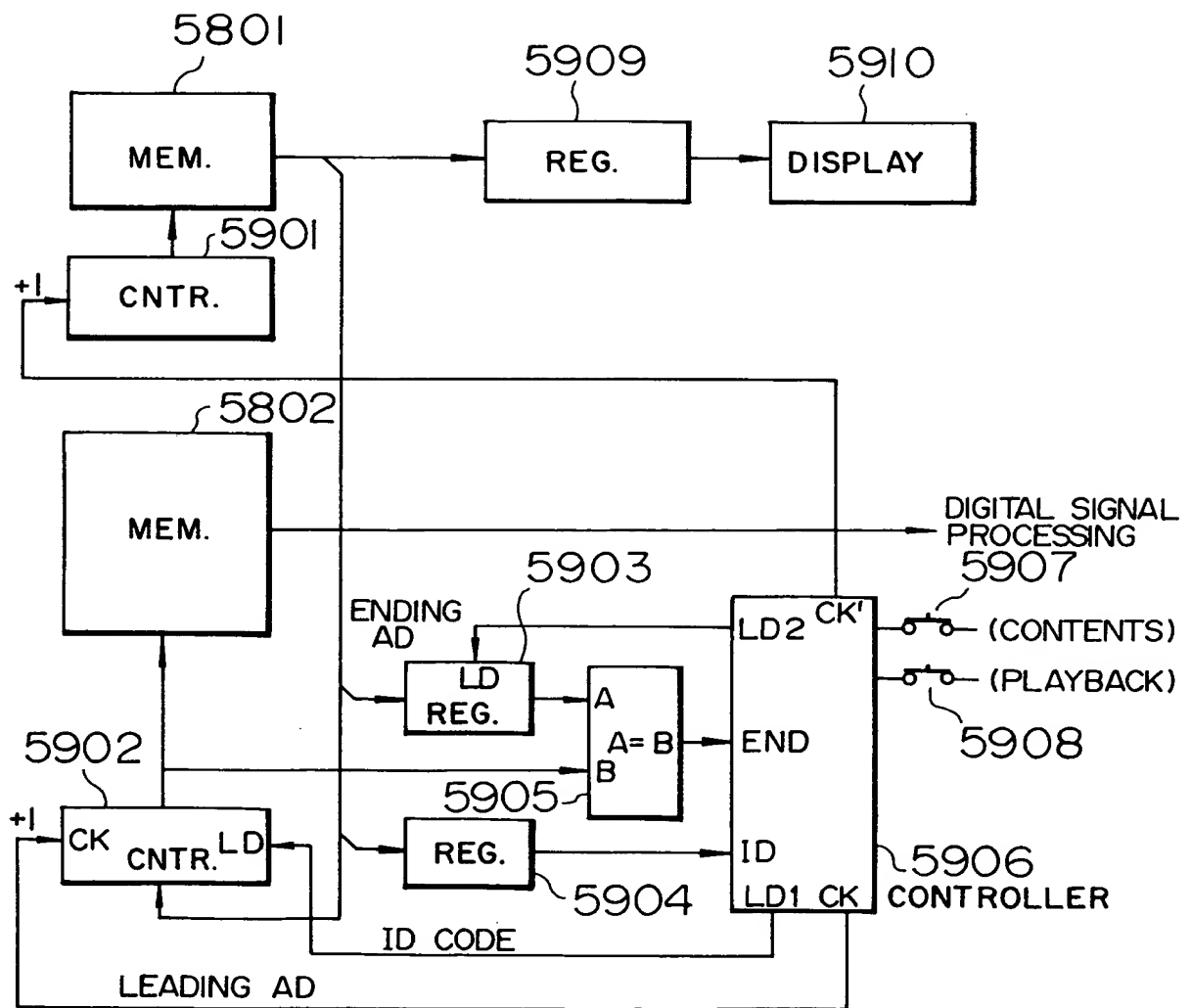
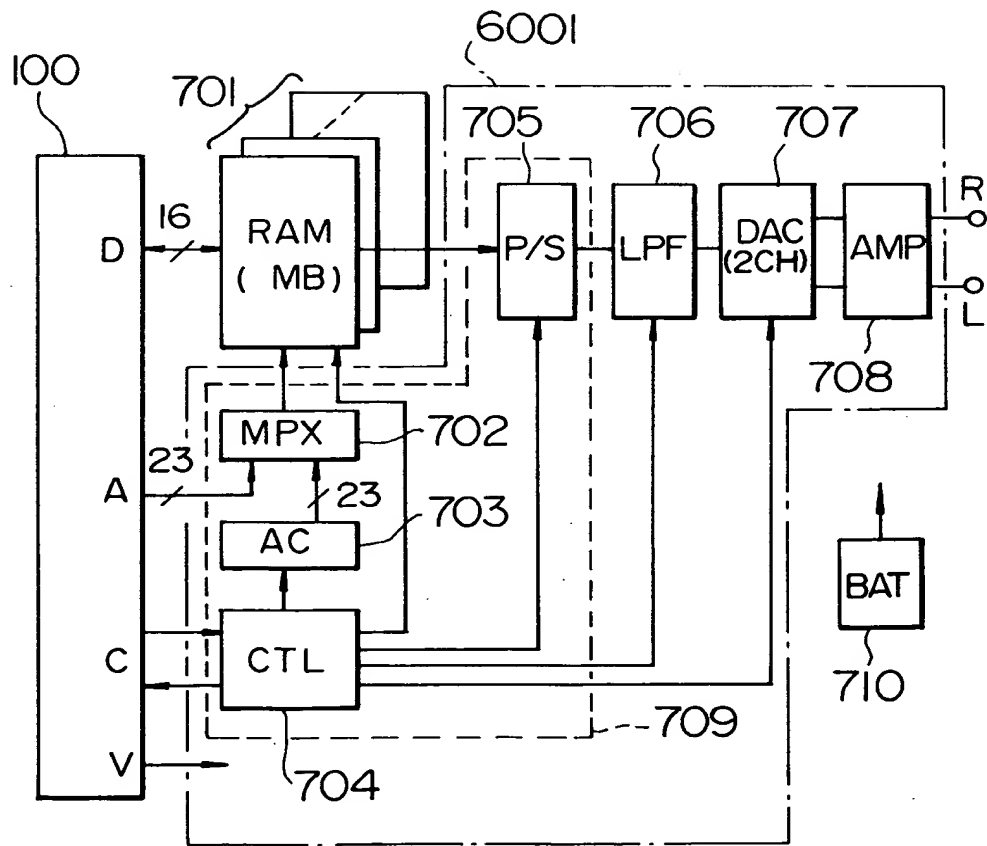


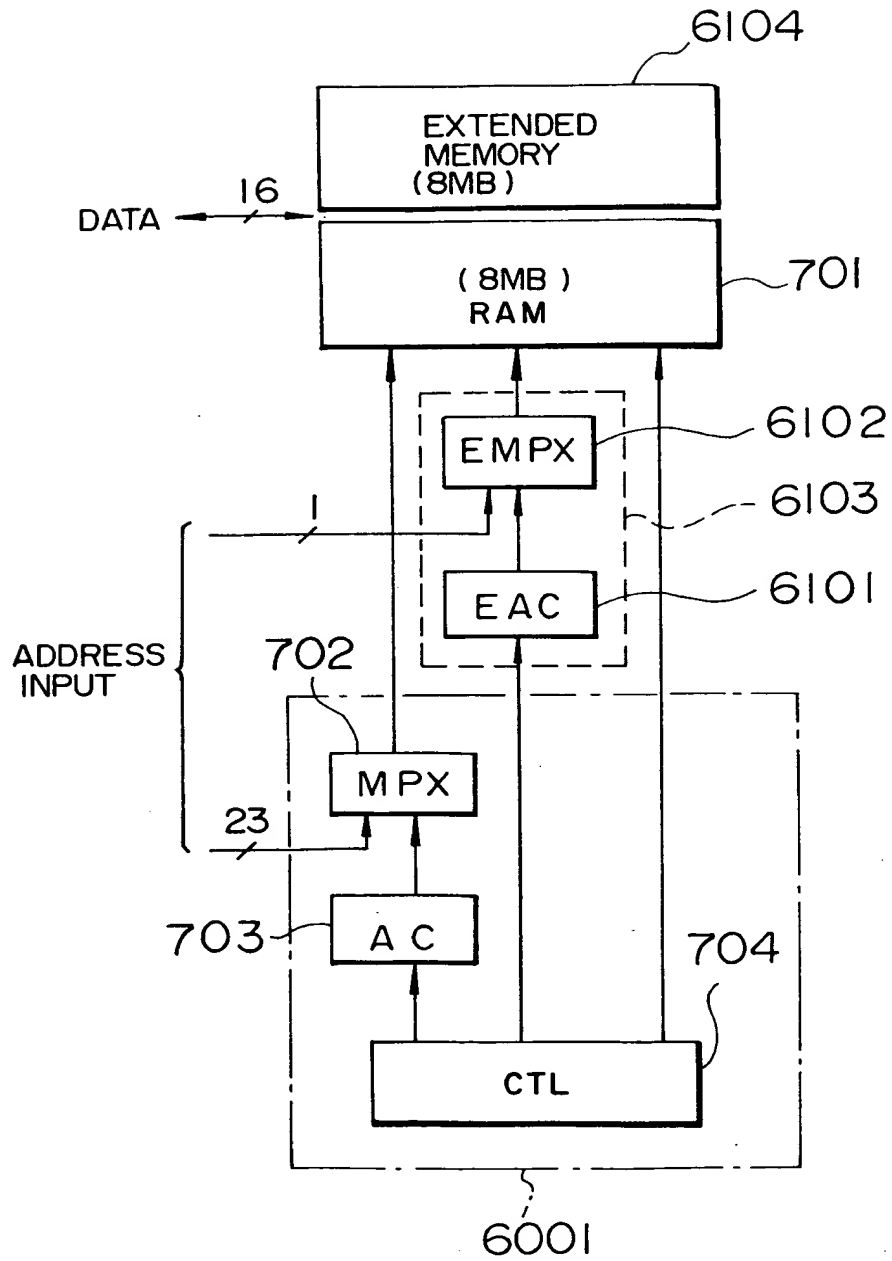
FIG. 60



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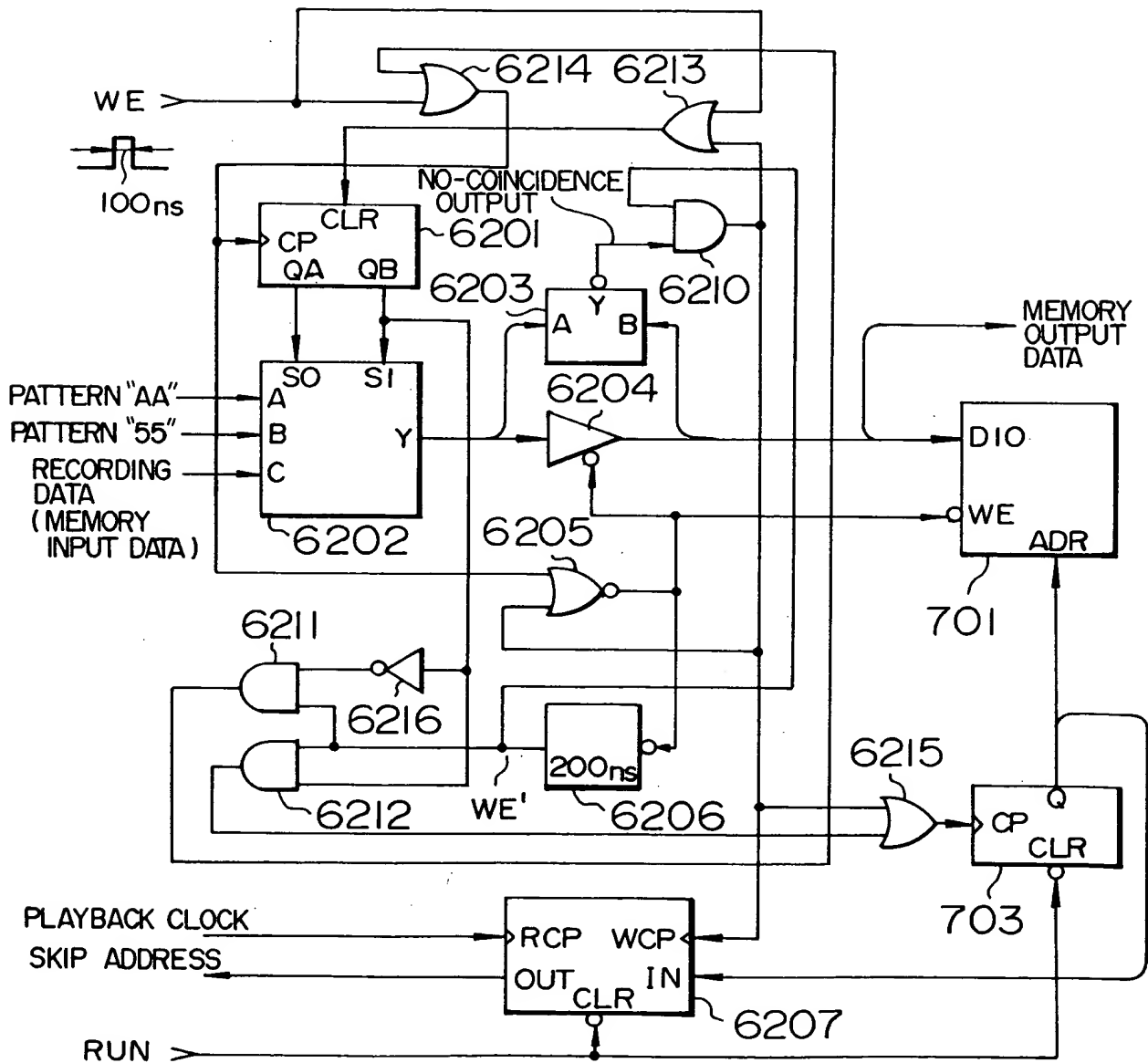
APPROVED	DATE	
BY	CLASS	SUBCLASS
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FIG. 6I



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FIG. 62

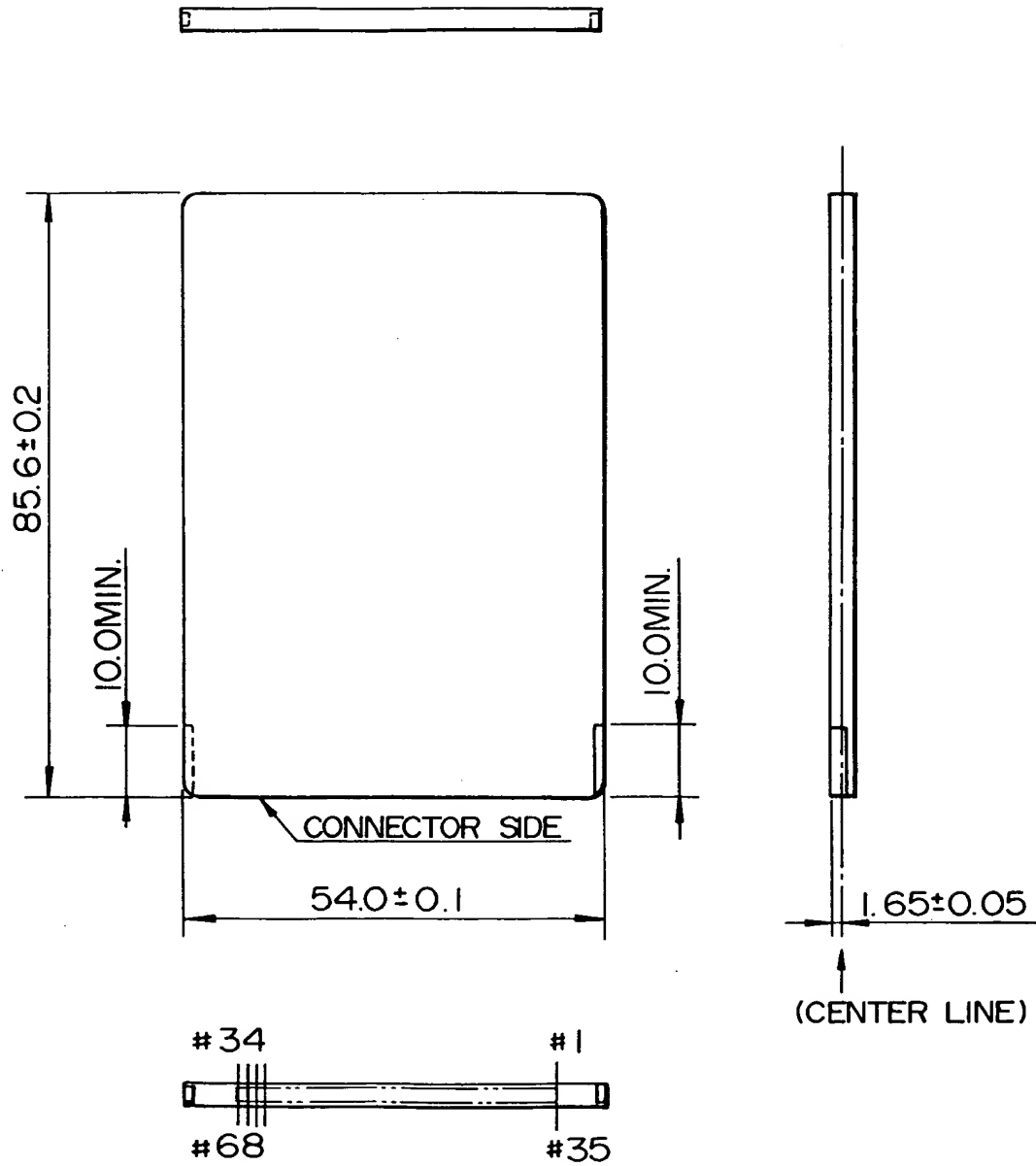


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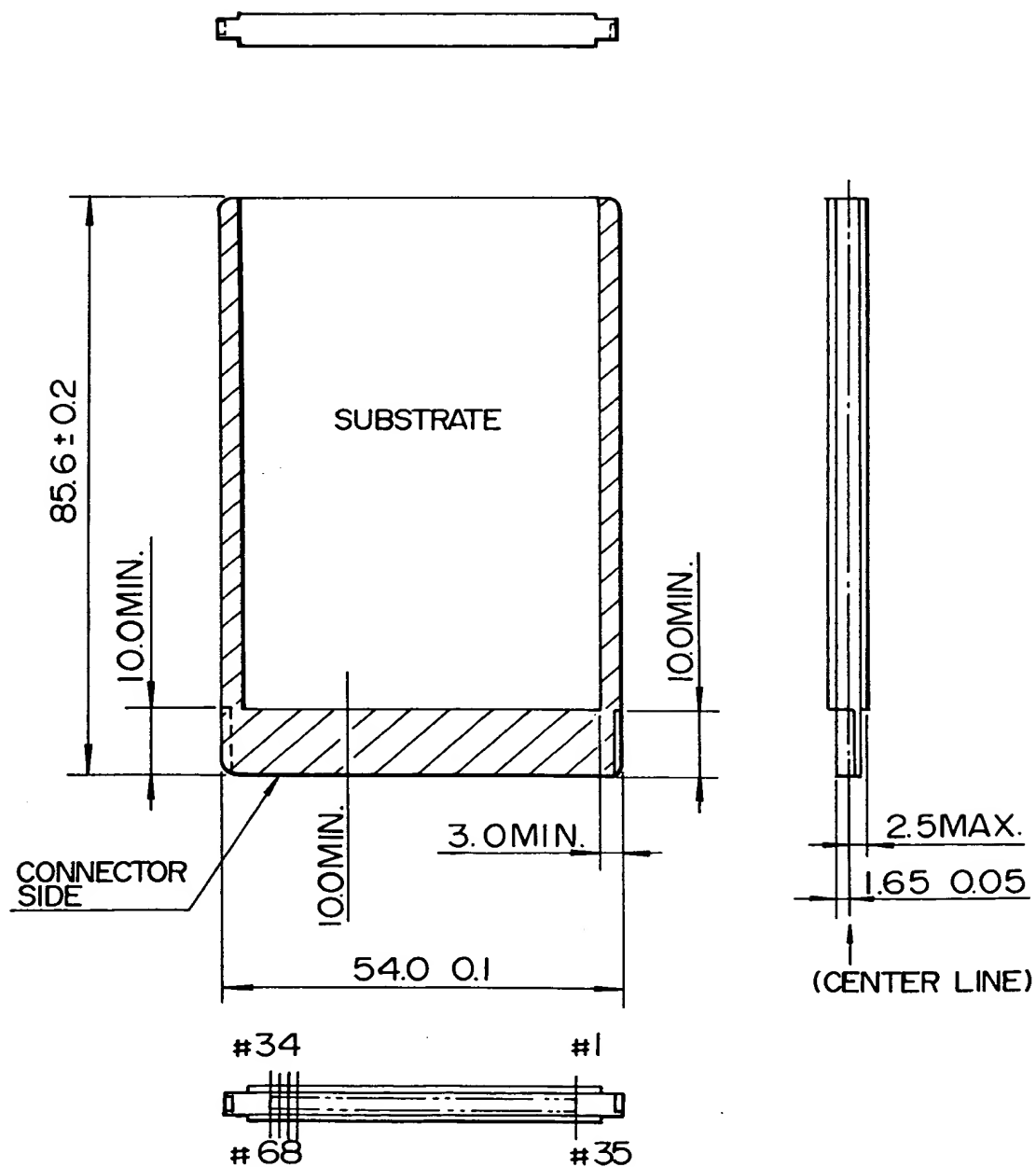
APPROVED	DATE	
BY	CLASS	SUBCLASS
DRAFTSMAN		

FIG. 63



APPROVED	DATE	FILE
BY	CLASS	SUBCLASS
DRAFTSMAN		

FIG. 64



102290" 89298860

# FIG.65

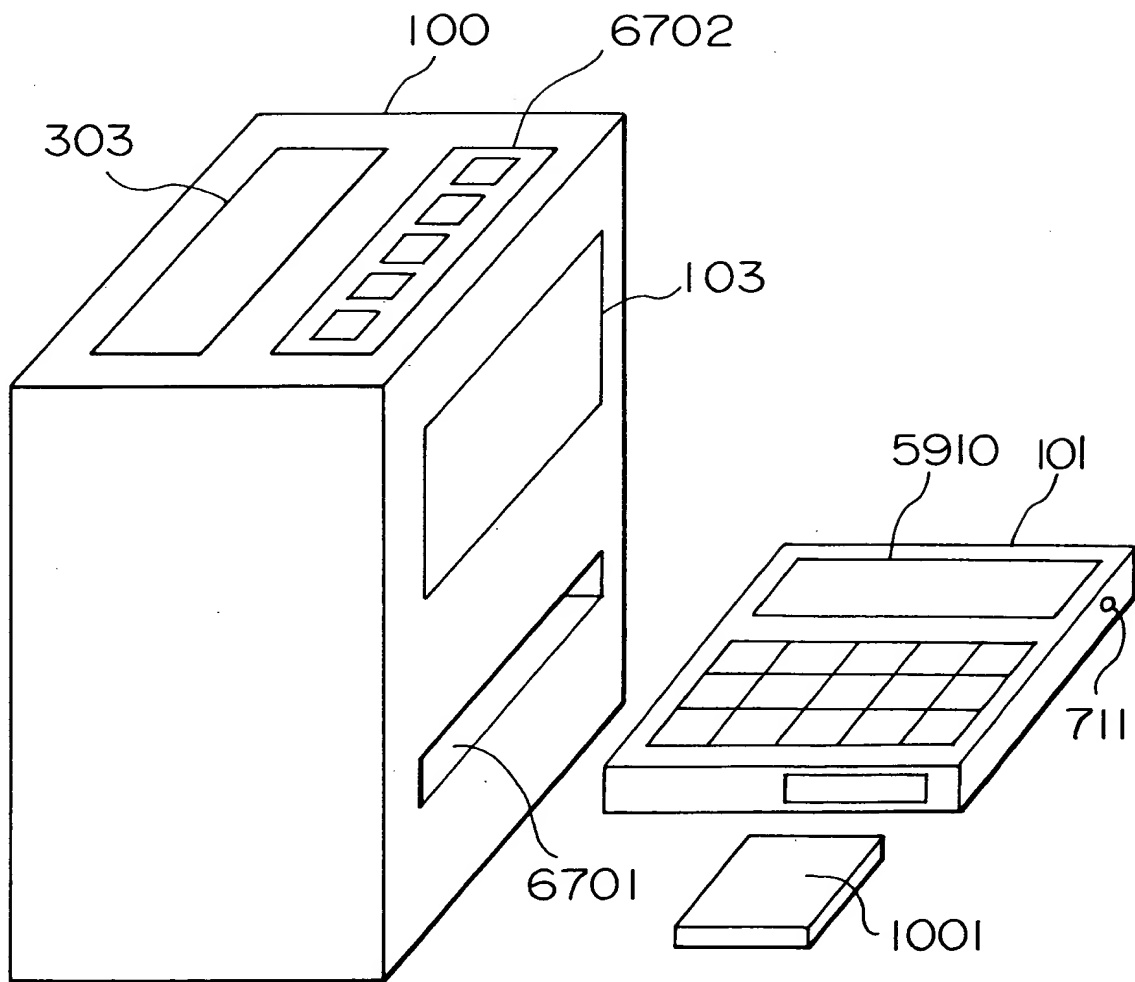
PIN	NAME	I/O	FUNCTION	PIN	NAME	I/O	FUNCTION
1	GND			35	GND		
2	D3	I/O		36	CD1	O	CARD DETECTION
3	D4	I/O		37	D11	I/O	
4	D5	I/O		38	D12	I/O	
5	D6	I/O		39	D13	I/O	
6	D7	I/O		40	D14	I/O	
7	$\overline{CE1}$	I	CARD ENABLE	41	D15	I/O	
8	A10	I		42	$\overline{CE2}$	I	CARD ENABLE
9	$\overline{OE}$	I	OUTPUT ENABLE	43	$\overline{RFSH}$	I	REFRESH ( FOR PSRAM )
10	A11	I		44	RFU	NC	RESERVE
11	A9	I		45	RFU	NC	RESERVE
12	A8	I		46	A17	I	
13	A13	I		47	A18	I	
14	A14	I		48	A19	I	
15	$\overline{WE}/\overline{PGM}$	I	WRITE ENABLE	49	A20	I	
16	RDY/ $\overline{BSY}$	O	RDY $\overline{BSY}$ (EEPROM)	50	A21	I	
17	VCC			51	VCC		
18	VPP1		PROGRAM POWER (EVEN-NUMBERED BYTES)	52	VPP2		PROGRAM POWER (ODD-NUMBERED BYTES)
19	A16	I		53	A22	I	
20	A15	I		54	A23	I	
21	A12	I		55	A24	I	
22	A7	I		56	A25	I	
23	A6	I		57	RFU	NC	RESERVE
24	A5	I		58	RFU	NC	RESERVE
25	A4	I		59	RFU	NC	RESERVE
26	A3	I		60	RFU	NC	RESERVE
27	A2	I		61	$\overline{REG}$	I	ATTRIBUTE MEMORY SELECTION
28	A1	I		62	BVD2	O	BATTERY VOLTAGE DETECTION
29	A0	I		63	BVD1	O	
30	D0	I/O		64	D8	I/O	
31	D1	I/O		65	D9	I/O	
32	D2	I/O		66	D10	I/O	
33	WP	O	WRITE PROTECT	67	$\overline{CD2}$	O	CARD DETECTION
34	GND			68	GND		

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FIG. 66

ITEM	SIGNAL	MEMORY CARD	SYSTEM	MEMORY CARD OUTPUT FORMAT
CONTROL SIGNAL	$\overline{\text{CE1}}$ $\overline{\text{CE2}}$ $\overline{\text{REG}}$	PULL UP TO VCC $R \geq 10K\Omega$	—	—
	$\overline{\text{OE}}$ $\overline{\text{WE/PGM}}$	PULL UP TO VCC $R \geq 10K\Omega$ , OR NO RESISTANCE	—	—
	$\text{RDY/BSY}$	—	PULL UP	NOT DETERMINED
	$\overline{\text{RFSH}}$	NC	—	—
ADDRESS	AO-A25	PULL DOWN TO GND $R \geq 100K\Omega$ , OR NO RESISTANCE	—	—
DATA BUS	DO-D15	PULL DOWN TO GND $R \geq 100K\Omega$ , OR NO RESISTANCE	—	THREE-STATE
CARD DETECTION	$\overline{\text{CD1}}$ $\overline{\text{CD2}}$	CONNECT CARD GND	PULL UP	CONNECT TO GND IN MEMORY CARD
WRITE PROTECTION	WP	—	—	"H" OR "L"
BATTERY VOLTAGE DETECTION	BVD1 BVD2	—	PULL UP	"H" OR "L"
RESERVE PIN	RFU	NC	NC	

FIG. 67



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FIG. 68

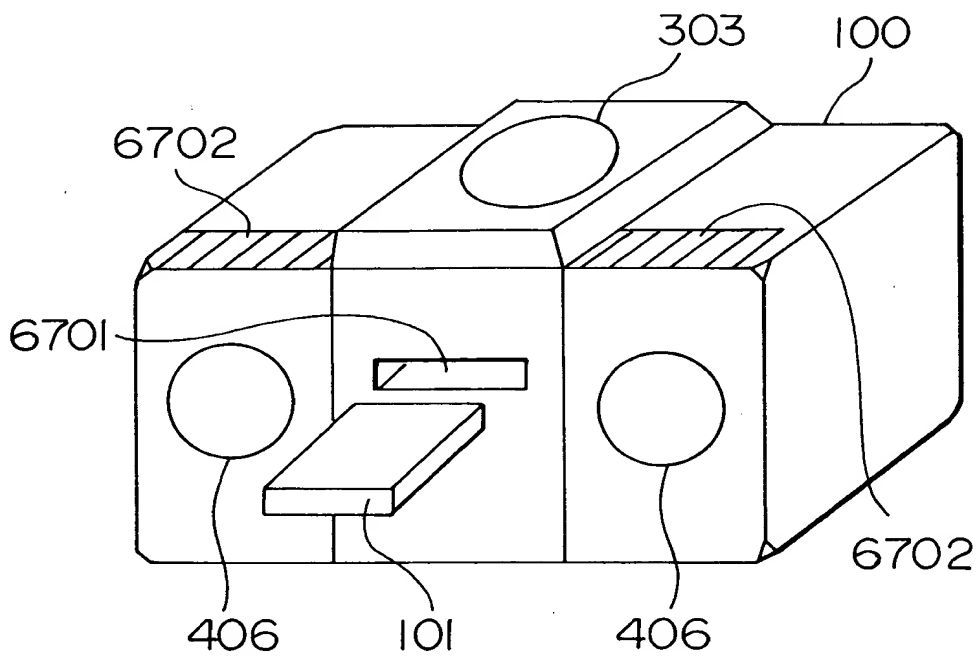
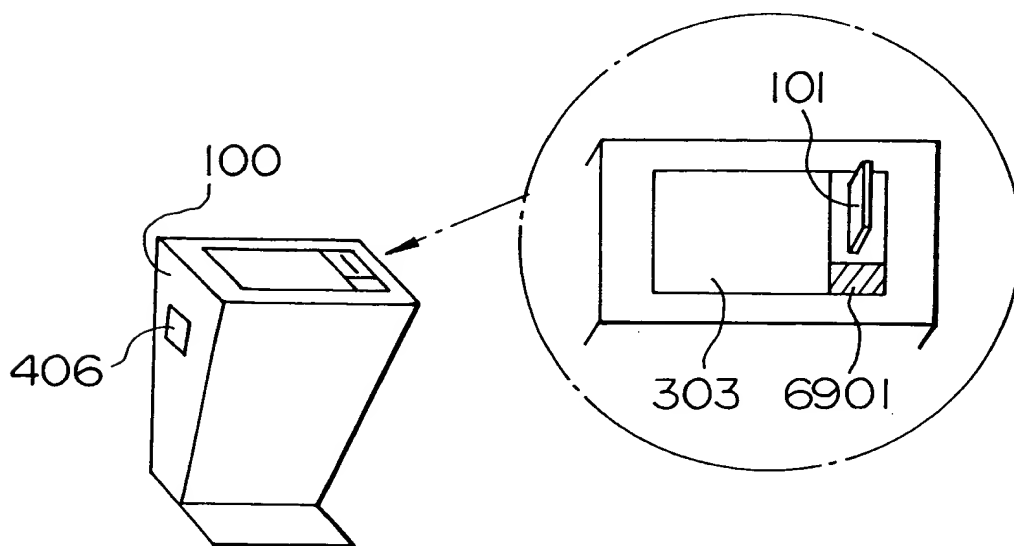


FIG. 69



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